A 310-GHz Fundamental Oscillator with 0.4-mW Output Power and 3.2% dc-to-RF Efficiency in 65-nm CMOS

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***Abstract*— This paper presents a 310-GHz fundamental oscillator with a differential T-embedding network. An on-chip transformer acts part of an embedding component and produces a single-ended output. The design is implemented in 65-nm CMOS process, occupying a core area of 0.01 μm^2. The oscillator generates 0.4-mW output power from two 16-μm transistor while drawing 10.39-mA current from a 1.2-V power supply, corresponding to a 3.2% dc-to-RF efficiency. To the best of the author's knowledge, this oscillator provides the highest fundamental frequency in CMOS with high output power and dc-to-RF efficiency.**

***Keywords*— fundamental oscillator, mm-wave, transformer, CMOS.**

I. Introduction

Millimeter-wave frequencies have found extensive applications in high data rate communication [1], automotive radars, imaging and spectroscopy [2]. Oscillators serve as a key block in almost all of these applications. The increasing demand for higher speed communication and better resolution in imaging/radar pushes operating frequency higher. Signal generation with adequate power and efficiency remains challenging especially in CMOS technology due to their relatively low f_{max} and high passive loss [3]–[5].

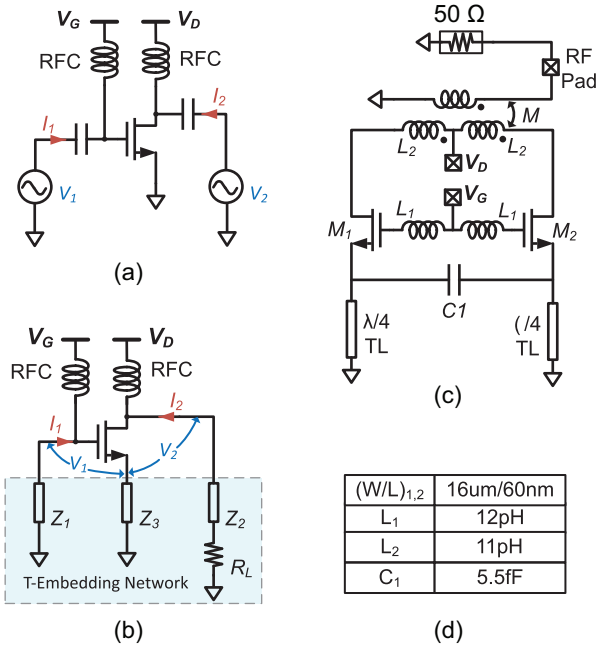
The performance of fundamental oscillators is critical in a sense that harmonic oscillators are designed based on them [6] and the maximum oscillating frequency reflects the f_{max} of a process [7]. Existing signal sources above 300 GHz are predominantly realized by harmonic oscillators or frequency multipliers [6], [8]–[11]. A 300 GHz fundamental oscillator [7] was demonstrated with very small transistor size (a total of 6.4μm of core oscillator) from which little output power can be extracted.

In this paper, we report a CMOS oscillator with a fundamental oscillation frequency of 310 GHz output power of 0.4 mW, and dc-to-RF efficiency of 3.2%. The proposed design utilizes a differential T-embedding network and output power is extracted by a on-chip transformer. Fig. 1(c) sketches the proposed design with the design parameters summarized in Fig. 1(d). This design achieves the highest operating frequency among fundamental oscillators in CMOS technology and the highest efficiency among >300-GHz integrated oscillators reported to date.

II. Design and Implementation

A. Design Theory

Fig. 1(a) shows the diagram of an active two-port network with voltage excitation [12]. If the two ports are excited with



$(W/L)_{1,2}$	16um/60nm
L_1	12pH
L_2	11pH
C_1	5.5fF

(d)

Fig. 1. (a) An active two-port network excited with two AC voltage source, (b) T-embedding network with load connected to drain, (c) Schematic of the proposed design, (d) Table of design parameters.

AC voltage sources V_1 and V_2, current response I_1 and I_2 can be obtained. The frequency of the AC source corresponds to the target oscillation frequency. To extract the maximum net output power (i.e. added power) of an active two-port network, the amplitude of V_1 and V_2 and their phase difference should be optimized. This could be done fairly easily in a modern EDA tool.

An oscillator is transformed from Fig. 1(a) into Fig. 1(b) by replacing the voltage sources with a embedding network. The oscillator is self-sustained by this feedback circuit that feeds a portion of the power from Port2 into Port1 with correct voltage and current phase. A general embedding network that satisfies optimal port voltage and current includes at least three independent passive embedding components and a load. In this case, the power delivered to the load will be same as the added power of a two-port network. To minimize the loss of a practical embedding network, we tend to use the simplest networks. Pi- and T-embedding networks are among the simplest candidates. In this work, T-embedding networks are selected due to easier differential design [13]. The embedding values can be synthesized by the following

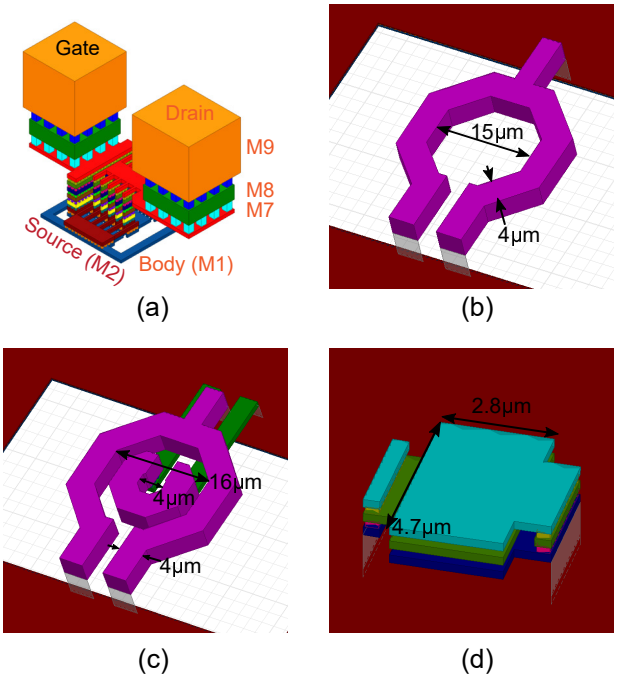


Fig. 2. The 3-D rendition of (a)16 μm NMOS transistor, (b) gate inductor L_1, (c) drain transformer, (d) source capacitor C_1.

equations assuming power is only dissipated at R_L [5]:

$$\begin{bmatrix} 0 & -I_{1I} & 0 & -(I_{1I}+I_{2I}) \\ 0 & I_{1R} & 0 & (I_{1R}+I_{2R}) \\ I_{2R} & 0 & -I_{2I} & -(I_{1I}+I_{2I}) \\ I_{2I} & 0 & I_{2R} & (I_{1R}+I_{2R}) \end{bmatrix} \begin{bmatrix} R_L \\ X_1 \\ X_2 \\ X_3 \end{bmatrix} = \begin{bmatrix} -V_{1R} \\ -V_{1I} \\ -V_{2R} \\ -V_{2I} \end{bmatrix} \quad (1)$$

where the subscript R and I denotes the real and imaginary part of port voltage and current V_i and I_i (i=1, 2).

The proposed oscillator is a differential design with two T-embedded oscillator directly coupled as shown in Fig. 1(c). The differential operation creates a virtual ground on the symmetry axis, and thus all the passive components which originally tied to ground can be combined in series. The differential operation provides a two-fold benefit for inductors: 1)differential configured inductors tend to show higher quality factor, 2) bias at the center tap of an inductor is less lossy than using a dc block capacitor. Capacitors in the embedding in differential configuration may be merged so that a smaller capacitor size could be used. In this design, since capacitors appear at the source of the transistor, a quarter-wave transmission line is placed at source to provide dc path. The transformer in conjunction with the 50 Ω load provides the same impedance as the series connection of Z_2 and R_L.

B. Implementation

The transistor used in this design is composed of two parallel 8-μm double-gate contact NMOS transistors [5]. Each 8-μm transistor consists of 10 fingers with 800-nm unit finger width. The size is chosen to balance the trade-off between output power and efficiency. While maximum added power from a transistor increases with total gate width, the resulting capacitor and inductor value decrease almost proportionally. The 16-μm transistor results in an embedding network where the Q of the inductor is highest at this frequency. A 3-D rendition of the transistor is shown in Fig. 2(a). The actual embedding network value used in this design is shown in Fig. 1(d). The 3-D view of all three passive components is shown in Fig. 2(b-d). The inductor and transformer are implemented with the 3.4-μm thick top metal for best quality factor. The diameter of the inductor is 15 μm with metal width of 4 μm. The EM simulated differential inductance and quality factor is 24.6 pH and 33, respectively. The two coils of the transformer are both implemented with top metal M9. The diamter of the outer and inner coil of the transformer is 16 μm and 4 μm, respectively. The diameter of inner coil is the result of 2-μm minimum line spacing from the DRC rule. The line width is 4 μm for both coils. The MOM capacitor is implemented with the top thin metals from Metal5 to Metal7. The capacitor is designed with a aspect ratio of 4.7 μm to 2.8 μm for best quality factor. The simulated capacitance and quality factor is 5.5 fF and 128, respectively.

III. Experimental Results

A picture of the fabricated circuit die is shown Fig. 3(a). The die size is 310 μm×210 μm. The core circuit occupies an area of 0.01 mm^2 excluding the dc and RF pads.

The measurement setup is similar to that in [5]. In the spectrum measurement, the LO signal from the N9030A spectrum analyzer is tripled and fed into a VDI WR-3.4 frequency extender. The extender internally multiply the LO signal by another 8 times. This signal is then mixed with the RF signal from a Cascade WR-3.4 probe. The down-converted IF signal enters the spectrum analyzer through a diplexer. The dc pads are connected to a off-chip low-dropout (LDO) regulator powered by batteries. Fig. 3(b) shows the measured IF spectrum with sweeping span of 10 GHz.

The output power is measured by a Erickson PM4 power meter. Between the power meter head and the WR-3.4 probe, a WR-3.4 S-bend and a taper from WR-10 to WR-3.4 is inserted. At 310 GHz, the loss of the RF probe, the S-bend and the taper are 6.5 dB, 2 dB and 0.5 dB, respectively. A total loss of 9 dB was compensated from the power meter reading.

The measured output power and efficiency is summarized in Fig. 4. At 1.2-V drain and 0.7-V gate bias, the oscillator draws 10.39 mA dc current and generates 0.4mW output power. The corresponding dc-to-RF efficiency is 3.2%. At 1.3-V drain and 0.8-V gate bias, the maximum output power of 0.5 mW is achieved with a dc-to-RF efficiency of 3.2%. Table 1 compares the measurement results with the state-of-the-art CMOS/SiGe oscillators around 300 GHz.

IV. Conclusion

This paper presents a 310 GHz differential T-embedding oscillator in 65-nm CMOS. The record-breaking performance is achieved by optimal T-embedding design and efficient

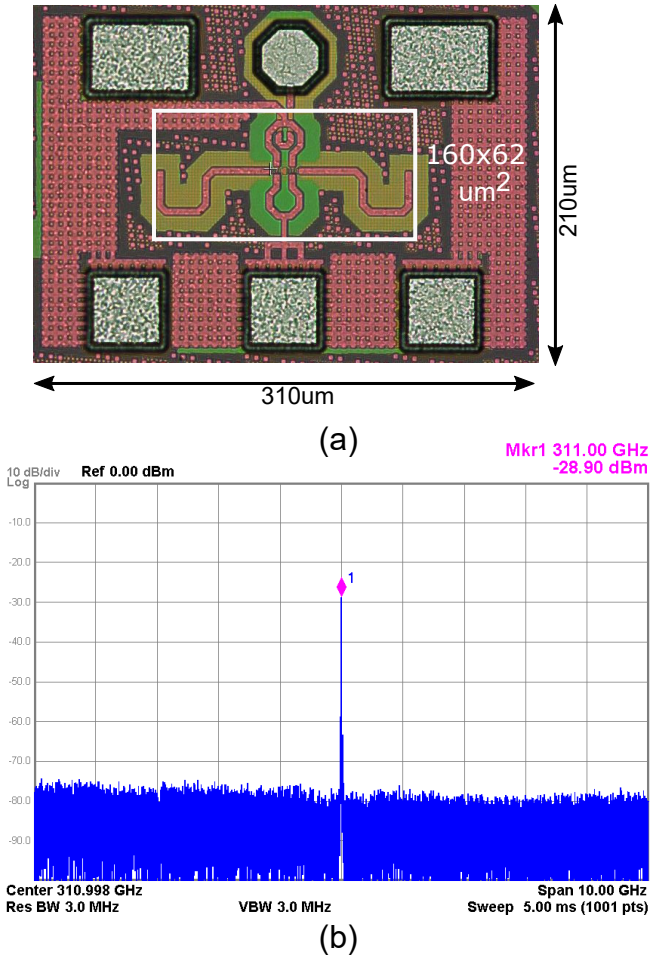


Fig. 3. (a) Fabricated circuit die photo. (b) Screen shot of measured spectrum of the oscillator

output balun. Such high frequency fundamental oscillator demonstrates the potential of CMOS process in the area of mm-wave circuits. Measurement results confirms the output power and efficiency of the 310 GHz oscillator.

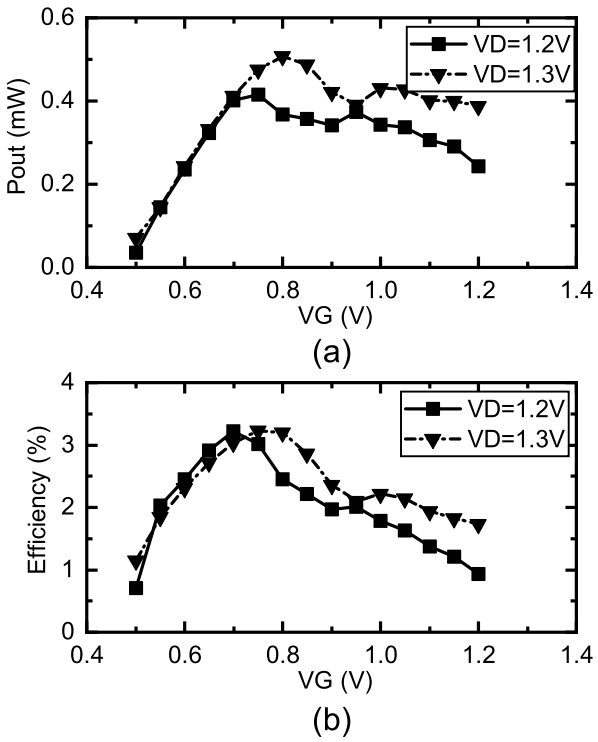


Fig. 4. (a) Measured output power (a) and efficiency (b) of the proposed oscillator versus gate and drain bias voltage

Table 1. Comparison with the State-of-the-Art

Metric	[7]	[14]	[3]	[15]	This Work
Technology	65-nm CMOS	130-nm SiGe	120-nm SiGe	32-nm CMOS	65-nm CMOS
Mode	Fund.	2-Push	2-Push	Fund.	Fund.
Frequency (GHz)	300	318	330	272	310
RF Power (dBm)	N/A	-2.2	-13.3	-22	-4
Phase Noise (dBc/Hz)†	N/A	-108	-78	N/A	-95
dc Power (mW)	3.7	142	63	7	13.3
dc-to-RF Efficiency (%)	N/A	0.8	0.07	0.09	3.2

† Specified at 10-MHz offset.

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