A 212-GHz Differential VCO with 5.3% dc-to-RF Efficiency in 65-nm CMOS Technology

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***Abstract*— This paper presents a 212-GHz fundamental VCO with a Π-embedding network with high dc-to-RF efficiency. Particle swarm optimization method is utilized to find the optimal values of elements of the lossy embedding network. Fabricated in 65-nm bulk CMOS, the VCO achieves 0.6-mW peak output power per transistor at 1-V power supply and the peak dc-to-RF efficiency of 5.3%. The measured phase noise is -92.5 dBc/Hz and -113.9 dBc/Hz at 1 MHz and 10 MHz offset, respectively. Bulk voltage is used as the tuning mechanism. The measured tuning rang is 212.2 GHz to 208.8 GHz when the bulk voltage is changed from 0 V to 0.8 V.**

***Index Terms*— fundamental oscillator, VCO, mm-wave, terahertz, CMOS.**

I. Introduction

The design of CMOS millimeter-wave (mmW) and terahertz (THz) signal sources with adequate output power and acceptable efficiency remains a challenge due to the limited maximum frequency of oscillation, f_{max}, of solid-state devices. Harmonic oscillators are specially designed when the operating frequency is close to or beyond f_{max} [1], [2]. In particular, fundamental oscillators are often preferred in that they can generate high power signals and there is no need of eliminating the harmonic output signals [3]–[6].

Oscillators with differential outputs are required for harmonic extraction [1], [7] and for differential circuits and systems [8]–[10]. A lossless embedding network is often assumed in designing high frequency (such as radio frequency, microwave frequency and mmW frequency) oscillators. However, in reality, the finite quality factor (Q) of passive elements of an embedding network has a significant effect on the oscillator performance. It results in shifting oscillation frequency, decreasing output power and increasing phase noise.

In this paper, we present a differential VCO using particle swarm optimization (PSO) based method which is able to quickly find the optimum values of elements of a lossy embedding. The proposed approach considers the nonlinearities of the transistor and the finite Q of the passive elements. It provides an accurate and optimal oscillator design in terms of the output power and dc-to-RF efficiency.

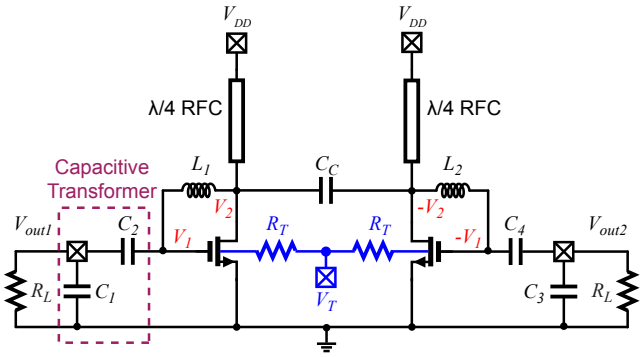

Fig. 1. Schematic of the 212-GHz fundamental differential VCO.

II. Design of the 212-GHz Fundamental VCO

A. Particle Swarm Optimization

In [3], a general methodology for designing high-efficiency mmW oscillators working close to f_{max} was presented. The approach is based on accurate nonlinear characterization of the active device and an analytical synthesis procedure for the design of the embedding networks with lossy on-chip passive components. Now due to the extra power loss in the passive components, the theoretical approach deviates from the actual optimal oscillation condition and design iterations and numerical optimizations were needed to finalize the design. In this work, we follow generally the same design procedure and elaborate on the PSO method.

We further investigate the effectiveness of this algorithm over a wider range of frequency and Q as a general solution for millimeter-wave oscillators. Fig. 3 plots the number of iterations of the algorithm over frequency and quality factors. The quality factor of inductors and capacitors are assumed to be the same in the simulation. Due to the random nature of the algorithm, the algorithm reaches convergence within a small variation of iterations for each run. The robustness of this method is confirmed by maximum number of iteration being always blew 30. In case of a brute force search, it would easily cost over 1000 simulations to reach moderate accuracy. Since only one

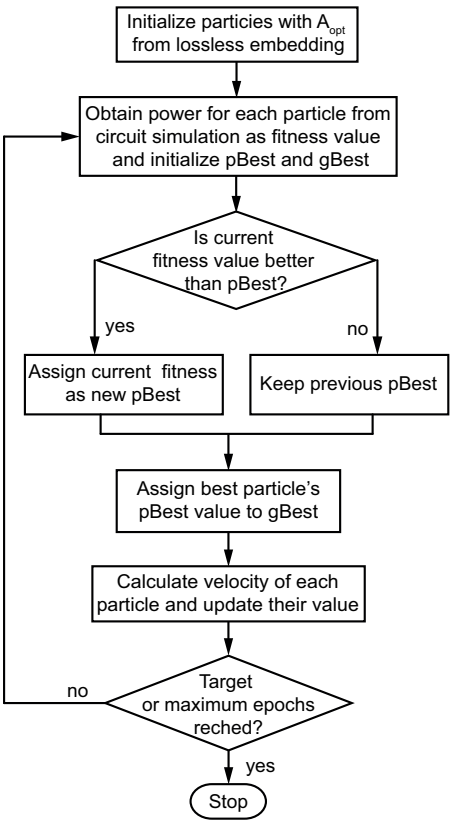

Fig. 2. Flow chart of the particle swarm optimization process

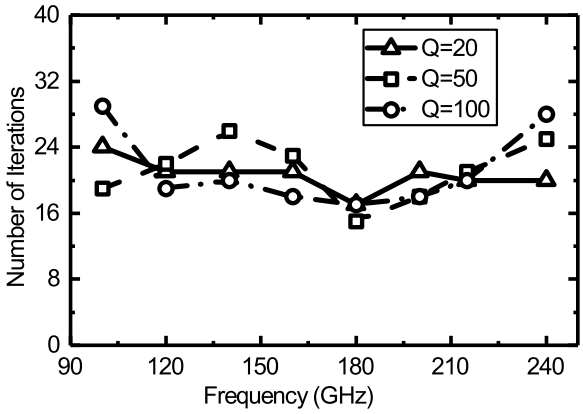

Fig. 3. Number of iterations over frequency with different quality factors

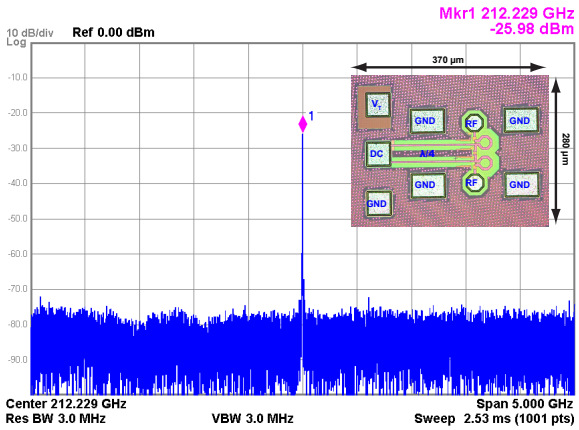

Fig. 4. Measured IF spectrum. Inset: Die photograph

circuit simulation is performed during each iteration per particle, the PSO based method is 15 times more efficient.

B. Implementation of the 212-GHz differential VCO

The differential output VCO consists of two identical fundamental VCOs locked 180° out-of-phase, which is realized by coupling two oscillator structures through the drain capacitor C_C at the fundamental mode, as shown in Fig. 1. Based on the large-signal Y-parameters of the transistor and the optimal complex voltage gain A which is obtained from PSO method, the calculated values of elements in Fig. 1 are $R_L = 50\,\Omega$, $C_1 = C_3 = 10.5$ fF, $C_2 = C_4 = 11.4$ fF, $C_C = 9.4$ fF, and $L_1 = L_2 = 32.8$ pH. The parasitic capacitance of the RF pads are used as C_1 and C_2. L_1 and L_2 are implemented using transmission lines. All of these values of passive elements are EM simulated results.

This 212-GHz fundamental differential VCO is implemented in a 65-nm bulk CMOS technology with nine metal layeres. 16-µm NMOS transistors are utilized. A deep n-well is used to isolate the MOS transistor's bulk. When bulk voltage is changed, the parasitic parameters of the transistor vary. Thus, frequency tuning can be realized by changing bulk voltage. The capacitors are constructed using top level metal (M6 and M7) parallel plates, which have high qualify factor. The transmission lines without underneath shield ground are used as inductors. In order to reduce the dc bias impact, the quarter-wavelength transmission lines are used to obtain high impedance (looking into bias pads) at drain. A micrograph of the fabricated VCO die is shown in Fig. 4. The differential VCO occupies 0.37 mm×0.28 mm including the pads.

III. Experimental Results

The measurement setups are the same as that used in [3]. To measure the differential VCO, both the signal analyzer and the power meter are connected to provide 50-Ω terminations to both ports. The output spectrum and output power are measured simultaneously.

The measured output spectrum of the differential VCO with bulk voltage $V_T = 0$ V is shown in Fig. 4. The oscillation frequency is 212.2 GHz. The measured output power, dc-to-RF efficiency, tuning range, and phase noise of the differential VCO are shown in Fig. 5(a–d).

This differential VCO draws total 22.74 mA dc current (for a single transistor, the dc current is 11.37 mA) from a 1.0 V supply. The single ended calibrated output power

TABLE I

COMPARISON WITH THE STATE-OF-THE-ART CMOS FUNDAMENTAL VCOS

Reference	Frequency (GHz)	RF Power (dBm)	Phase Noise (dBc/Hz)	dc Power (mW)	dc-to-RF Efficiency (%)	Technology
[11]	210	-13.5	-81.0 @1 MHz	42	1.5	32-nm CMOS SOI
[12]	240	-7	-93.0 @10 MHz	13	1.5	32-nm CMOS
[13]	219	-3	-77.4 @1 MHz	24	2.08	65-nm CMOS
[4]	213	-2.5	87.0 @1 MHz	14.35	3.9	65-nm CMOS
This work	212	-2.21	-92.5 @1 MHz	11.37	5.3	65-nm CMOS

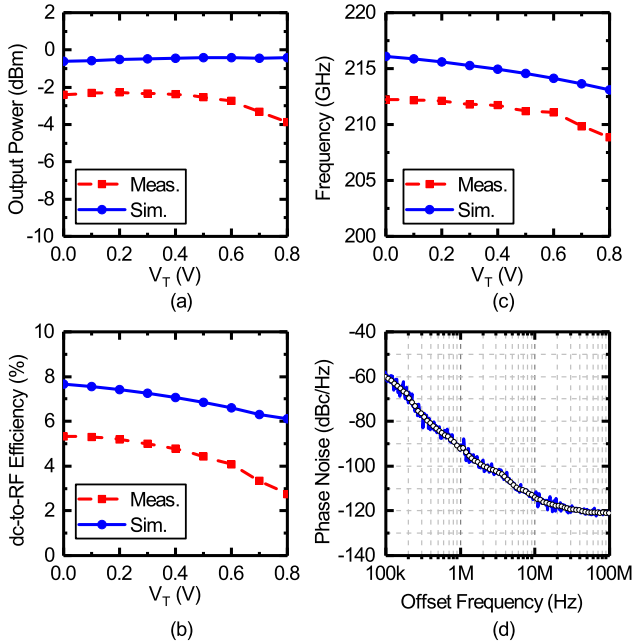

Fig. 5. Measured (dash lines) and simulated (solid lines) performance of the VCO. (a), (b), (c) and (d) show the output power, dc-to-RF efficiency, tuning range and phase noise of the designed VCO when V_{DD} is 1.0 V. In the simulations, all passive elements are extracted using 3D electromagnetic simulations.

is 0.6 mW and it achieves 5.3% dc-to-RF efficiency. The measured tuning rang is 212.2 GHz to 208.8 GHz when the bulk voltage is changed from 0 V to 0.8 V. The measured phase noise is -92.5 dBc/Hz and -113.9 dBc/Hz at 1 MHz and 10 MHz offset, respectively.

IV. CONCLUSION

In this work, we present a 212-GHz differential VCO implemented in a 65-nm CMOS technology. The PSO optimization approach is used to obtain the complex voltage gain A. Bulk voltage is used as the tuning mechanism. The tuning rang is 212.2 GHz to 208.8 GHz when the bulk voltage is changed from 0 V to 0.8 V. This VCO achieves 5.3% dc-to-RF efficiency with 0.6-mW output power per transistor and phase noise of -92.5 dBc/Hz and -113.9 dBc/Hz at 1 MHz and 10 MHz offset, respectively.

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