# A Compact 213 GHz CMOS Fundamental Oscillator with 0.56 mW Output Power and 3.9% Efficiency using a Capacitive Transformer

Hao Wang, Daniel Kuzmenko, Bo Yu, Yu Ye, Jane Q. Gu, Hooman Rashtian, Xiaoguang Liu
University of California Davis
haowang@ucdavis.edu, lxgliu@ucdavis.edu

***Abstract*—This paper presents a compact 213 GHz fundamental oscillator with an optimal embedding network that maximizes the output power. Fabricated in 65-nm bulk CMOS, the oscillator occupies a core area of only $70\times40\,\mu m^2$, owing to the use of a compact low-loss capacitive transformer structure. The oscillator achieves 0.56-mW output power while consuming a DC current of 14.35 mA from a 1-V power supply, representing a recording-breaking DC-to-RF efficiency of 3.9% amongst fundamental oscillators above 200 GHz.**

***Index Terms*—fundamental oscillator, mm-wave, terahertz, compact signal generator, CMOS**

## I. Introduction

CMOS circuits are gaining increasing attentions in microwave, millimeter wave, and THz frequency band (sub-millimeter wave). As the operating frequencies approaches the maximum frequency of oscillation $f_{max}$ of the devices, power generation with high power efficiency has become every more challenging.

In recent years, significant progress has been made in the use of high-speed integrated circuits for the generation of millimeter-wave and THz signals [1]–[5]. Harmonic oscillators and power combining are popular approaches to generate relatively high power signals beyond 200 GHz.

In this paper, a compact 213 GHz fundamental oscillator and its design methodology is introduced. Fig. 1 captures the concept of the proposed design. Most notable is the use of compact capacitive transformer inside an optimal embedding network around a high-speed active device. The proposed oscillator achieves record breaking performance in terms of power efficiency in the smallest footprint reported to date.

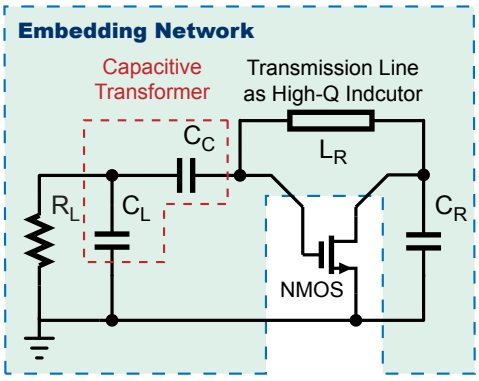


Fig. 1. Schematic of the proposed 213-GHz oscillator

## II. Theory and Design

### A. Achieving Maximum Output Power

The theory for predicting the maximum oscillation output power of an active device has been developed previously by several works [6]–[8] and will be briefly summarized here.

Let $y_{ij} = g_{ij} + jb_{ij}$ denote the large-signal Y-parameters of a non-linear active two-port network as shown in Fig. 2(a). Let $V_1$ and $V_2$ be the complex voltages at port 1 and 2 of the two-port network. A complex voltage gain $A$ is defined as

$$A = A_R + jA_I = \frac{V_2}{V_1}.$$

The output power flowing from the two-port network is defined as

$$P_R = -\frac{1}{2}|V_1|^2 [g_{11} + g_{22}(A_R^2 + A_I^2) + A_R(g_{12} + g_{21}) - A_I(b_{12} - b_{21})].$$

The complex voltage ratio $A$ can be optimized by keeping $V_1$ constant while varying both the magnitude and phase of $V_2$ until the real power $P_R$ flowing out of the nonlinear active device is a maximum. For the maximum value of $P_R$, the optimum complex voltage gain $A_{opt}$ can be found

$$A_{opt} = -\frac{y_{21} + y_{12}^*}{2g_{22}}.$$

In essence, the optimization of the output power of an active network is equivalent to finding the optimal embedding network that allows $A_{opt}$ to be realized.

### B. Extraction of Transistor Parameters

To calculate $A_{opt}$, we need to extract the network parameters of the underlying active devices. In this work, we realize our design in a 65-nm bulk CMOS process. To achieve a high

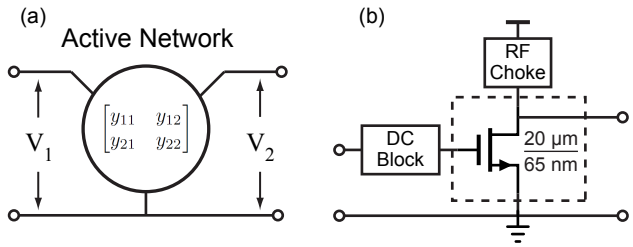


Fig. 2. (a) A general nonlinear active two-port network. (b) Two-port simulation setup for extracting the large-signal Y-parameters of the NMOS transistor.

$f_{max}$, we custom lay out a 20-µm NMOS transistor, as shown in Fig. 3(a). This transistor is constructed using two parallel 10-µm NMOS transistors. Double gate contacts are used to increase $f_{max}$ by reducing the gate input resistance. A 3-D rendition of the interconnects to the transistor is shown in Fig. 3(b).

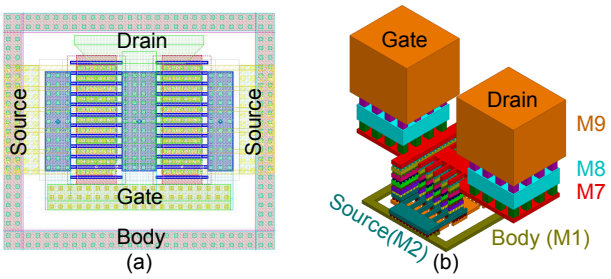


Fig. 3. (a) Layout of the 20-µm NMOS transistor (b) Interconnect setup used for connecting to the transistor.

The extracted transistor is placed in a common source configuration (Fig. 2(b)) to extract its large-signal Y-parameters, which are then used to calculate $A_{opt}$. Fig. 4 shows that the magnitude and phase of $A_{opt}$ both decrease with respect to frequency. At 213 GHz, the optimum amplitude of $A_{opt}$ is 1.77 and the optimum phase is 161.86°.

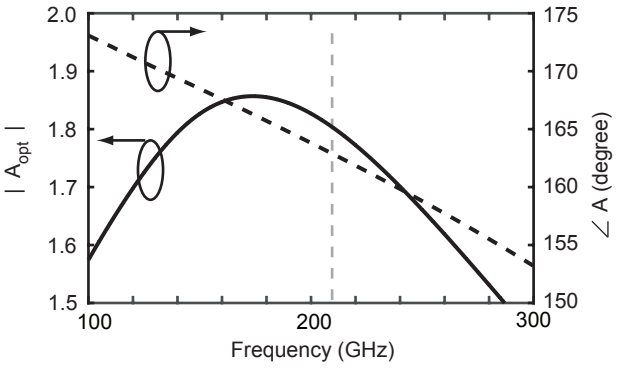


Fig. 4. Simulated optimum complex voltage gain $A_{opt}$.

### C. Oscillator Topology

The next step in the design process is to chose an external circuit that facilitates the realization of above calculated $A_{opt}$. In [8], various types of embedding networks have been investigated. Among them, the Y-oscillator model (Fig. 5(a)) stands out as an optimal convenient choice for the specific technology and transistor structure used in this work, as it allows easily realizable component values for millimeter-wave frequencies.

Specifically, Fig. 5(b) shows the chosen topology of our initial design. The embedding network consists of three reactive components $B_1$, $B_2$, $B_3$. The load, denoted by $G_1(R_1)$, is connected in parallel with $B_1$ between the gate and source terminals of the NMOS device. In this figure, the biasing networks to the transistor has been omitted for clarity.

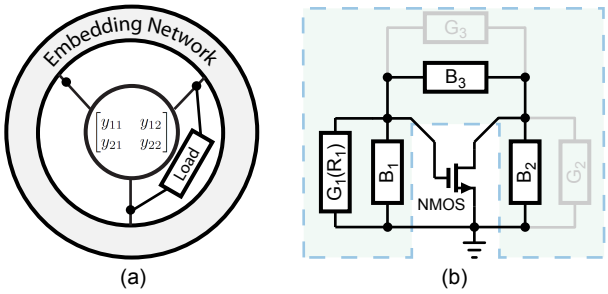


Fig. 5. (a) A conceptual representation of the Y-oscillator model. (b) Initial oscillator topology for optimal output power.

In general, the embedding network parameters can be obtained by solving the following linear matrix and specifying two of the six unknowns $(G_1, G_2, G_3, B_1, B_2, B_3)$ [7]:

$$\begin{bmatrix} 1 & 0 & 1-A_R & 0 & 0 & A_I \\ 0 & 0 & -A_I & 1 & 0 & 1-A_R \\ 0 & A_R & A_R-1 & 0 & -A_I & -A_I \\ 0 & A_I & A_I & 0 & A_R & A_R-1 \end{bmatrix} \begin{bmatrix} G_1 \\ G_2 \\ G_3 \\ B_1 \\ B_2 \\ B_3 \end{bmatrix} = \begin{bmatrix} -g_{11} - \Re(Ay_{12}) \\ -b_{11} - \Im(Ay_{12}) \\ -g_{21} - \Re(Ay_{22}) \\ -b_{21} - \Im(Ay_{22}) \end{bmatrix}$$

In the chosen topology, $G_2$ and $G_3$ should theoretically be set to zero. Therefore, this matrix reduces to four linear equations which can be solved for the embedding admittance parameters. The resulting component values for optimal oscillation at 213 GHz are as follows: $G_1 = 0.0156$, $B_1 = 0.0896$, $B_2 = 0.0509$, $B_3 = -0.0508$.

In practice, however, the finite Q of reactive components at millimeter-wave frequency cannot be neglected. In the design of this oscillator, component values are adjusted around their theoretical optimal values—without changing the resonant frequency—to ensure proper start of oscillation. The final design values of the embedding network are: $C_1$ =5.71 fF (corresponding to $B_1$), $C_2$ = 20 fF (corresponding to $B_2$), $L$ =26.27 pH (corresponding to $B_3$), $R_1$ =98 Ω (corresponding to $G_1$).

### D. Capacitive Transformer

We take advantage of the parallel connection between $R_1$ and $C_1$, and utilize a capacitive transformer to match a typical system impedance of 50 Ω to $R_1$ =98 Ω. Compared to inductor transformers, a significant advantage of the capacitive transformer is that it requires much less area.

It is straightforward to calculate the required capacitors $C_L$ =8.0 fF and $C_C$ =20.0 fF based on $R_1$, $C_1$, and $R_L$ =50 Ω using (1) and (2). Fig. 1 captures the final schematic of the oscillator design.

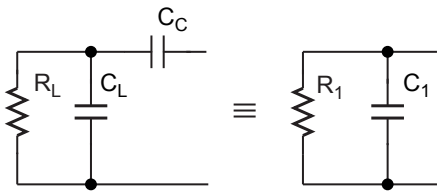


Fig. 6. (a) Capacitive transformer (b) Equivalent circuit of the transformer

$$C_L = C_1\sqrt{\frac{R_1}{R_L}}, \tag{1}$$

$$C_C = C_1\left(1 + \frac{1}{\sqrt{\frac{R_1}{R_L}} - 1}\right). \tag{2}$$

### *E. Implementation Details*

The three capacitors ($C_L$, $C_C$, and $C_R = C2$) are implemented by Metal-Oxide-Metal(MOM) capacitors constructed betwen M6 and M7. The inductor $L_R = L_3$ is implemented by a 71-µm long microstrip transmission line. The effective quality factor of the inductor implementation is 19.9 at 213.0 GHz. A quarter wavelength (at 213 GHz) transmission line is connected between the DC pad and the drain of the transistor as an RF choke. All passive components are designed using full-wave electromagnetic simulation.

## III. Experimental Results

The micrograph of the fabricated circuit die is shown in the inset of Fig. 7. The die size is $0.26 \times 0.26\,\text{mm}^2$. Owing to the use of capacitive transformer, the core size of the oscillator is only $70 \times 40\,\mu\text{m}^2$, at least 5 times smaller than the smallest reported oscillators at comparable frequencies.

The output spectrum (Fig. 7) of the oscillator is measured using a spectrum analyzer (Agilent N9030A) with an external OML harmonic mixer. The output power of the oscillator is measured with an Erickson PM4 calorimeter. With DC current of 14.35 mA from a 1-V power supply, this oscillator achieves 0.56 mW peak output power with 3.9% DC-to-RF efficiency. To the best of the authors' knowledge, this represents the highest efficiency among all reported fundamental oscillators above 200 GHz. Table I compares this oscillator with the state-of-art and shows clearly the advantages of our proposed design in terms of efficiency and area.

## IV. Conclusion

This paper presents a high efficiency 213-GHz fundamental oscillator in a 65-nm bulk CMOS process and its design methodologies. Owing to the use of optimal embedding network topology and compact capacitive transformers, the reported oscillator achieves record breaking efficiency levels and the smallest footprint among integrated fundamental oscillators with an output frequency above 200 GHz.

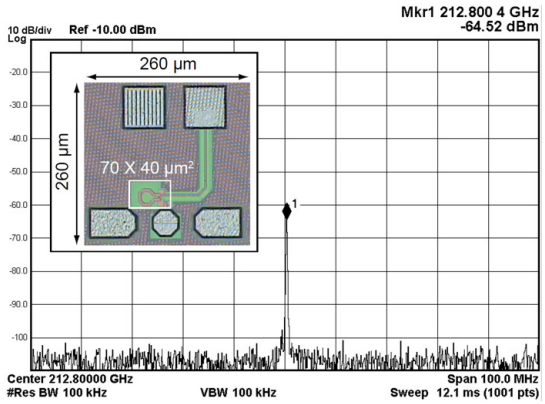


Fig. 7. Screen capture of the spectrum measurement of the fabricated oscillator. Inset: Die photograph.

TABLE I
Comparison with other State-of-the-Art Integrated Oscillators

| | [2] | [3] | [4] | [5] | This work |
|---|---|---|---|---|---|
| Frequency (GHz) | 210 | 219 | 236 | 210 | 213 |
| RF Power (dBm) | 1.4 | -3 | -3.6 | -13.5 | -2.5 |
| DC Power (mW) | 26 – 61 | 24 | 54 | 42 | 14.35 |
| DC-to-RF Efficiency | 2.4% | 2.08% | 0.81% | 0.1 | 3.9% |
| Phase Noise(dBc/Hz) | -87.5 @1 MHz | -77.4 @1 MHz | -98 @10 MHz | -81 @1 MHz | -87 @1 MHz |
| Area ($mm^2$) (Chip/Core) | 0.08 / 0.027 | 0.105 / 0.014 | NA | NA / 0.04 | 0.067 / 0.0028 |
| Technology | 130-nm SiGe | 65-nm CMOS | 130-nm SiGe | 32-nm SOI | 65-nm CMOS |

## V. Acknowledgment

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