Microstrip Line based Sub-THz Interconnect for High Energy-Efficiency Chip-to-Chip Communications

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Abstract — This paper presents sub-THz interconnect for high energy-efficiency chip-to-chip communications, including a microstrip line based low-loss wideband sub-THz channel and a high energy-efficiency transceiver. The channel loss is as low as 0.06 dB/mm. The transmitter output power is 0.66 dBm with 8.8 mW of DC power consumption, and the receiver consumes 60.8 mW DC power. The interconnect achieves 9-Gb/s on-off keying data transmission with a bit-error rate of less than 10^{-12} and an energy efficiency of 7.7 pJ/bit.

Keywords—Channel; interconnect; micromachined; microstrip line; sub-THz; THz; transceiver

I. Introduction

As rapid growth of demands of scientific workloads and commercial applications, the I/O bandwidth requirement is increased about twice per two years [1]. However the I/O pin number increases slowly due to physical limitations, such as pad size, cross talk issue. Besides, the energy for data communications needs to drop in a rate proportional to the data rate increasing to sustain the trend. Therefore, to ultimately solve the problem of intra-/inter- chip interconnect, both bandwidth density and energy efficiency should be boosted.

There are two major research areas for high speed interconnect: electrical interconnect [2], [3], and optical interconnect [4]. Electrical schemes, include baseband wireline, wireless, are compatible with existing planar silicon processes. For the wireless chip-to-chip communication, it has the configuration flexibility. However, it suffers from the large path loss which is inversely proportional to λ^2, and causes large channel coupling. For the baseband wireline interconnect, it has high data rate due to mature design methods. However, the bandwidth density is restricted due to the limited I/O pin number. On the other hand, the optical schemes, such as fiber, optical waveguide, provide high bandwidth and low loss. However, the challenge for the optical schemes is to integrate the optical channel with planar CMOS processes.

This paper presents microstrip line (MSL) based RF wireline interconnect as shown in Fig. 1. With the low-loss passive channel and low-power active chips, the energy efficiency is improved significantly. Besides, thanks to the modulated RF signal instead of baseband signal, the bandwidth density would be improved as well. To prove the concept and the functionality, the system is designed and optimized at G-band The low-loss wideband channel is micromachined on quartz substrate and the high energy-efficient transceiver chips are implemented in a TSMC 65 nm bulk CMOS process.

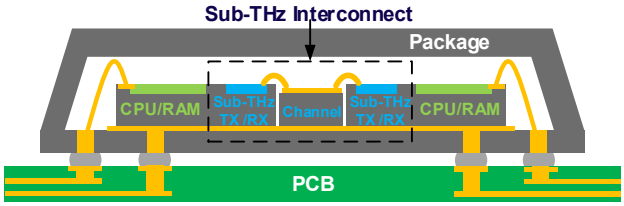

Fig. 1. Proposed MSL based sub-THz interconnect.

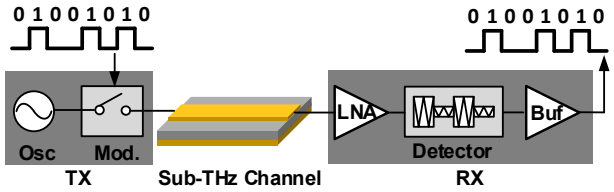

Fig. 2. Top block diagram of MSL based sub-THz interconnect.

II. Design of Sub-THz Interconnect

The top block diagram of the sub-THz interconnect is shown in Fig. 2. It consists of a cross-coupled oscillator, a switch based modulator, a MSL line based sub-THz channel, a 3-stage cascaded low noise amplifier (LNA), an envelope detector (ED) based demodulator, and a limiting amplifier (LA) based output buffer. Due to the low-loss channel, the link path loss is low, and the power amplifier-free architecture is adopted to boost the energy efficiency.

The channel is implemented with a MSL on a quartz substrate ($\varepsilon_r = 3.78$, $\tan\delta = 0.0002$). For 100-μm substrate, the line width $w = 216$ μm for the 50-Ω characteristic impedance. The signal is excited through a coplanar waveguide (CPW), and transitioned to a MSL. To simplify the fabrication, a via-free CPW to MSL transition is adopted. A quarter wavelength open single stub is chosen for ground pads is to provide the AC ground. The simulated minimal insertion loss is 0.5 dB for 8.1-mm MSL with CPW transitions on full-wave simulation in ANSYS high frequency structure simulator (HFSS).

Figure 4 shows the transmitter schematic, which consists of a transformer based impedance boosting fundamental signal

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generator and a high-speed high on-off ratio single-pole and single-throw (SPST) switch based on-off keying (OOK) modulator [5]. The transformer is employed to tune the oscillation frequency and boost the output impedance. The boosted impedance allows small transconductance g_m or transistor size to reduce power consumption and parasitics for high DC-to-RF efficiency.

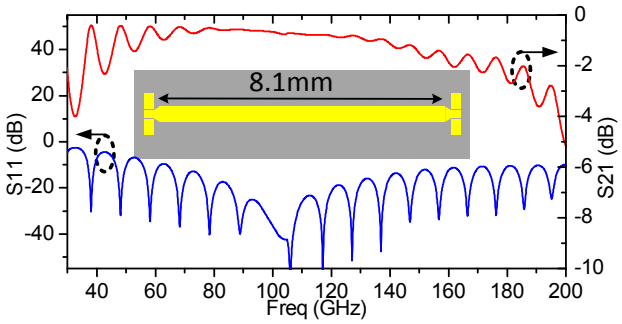

Fig. 3. Simulated and measured sub-THz interconnect channel S-

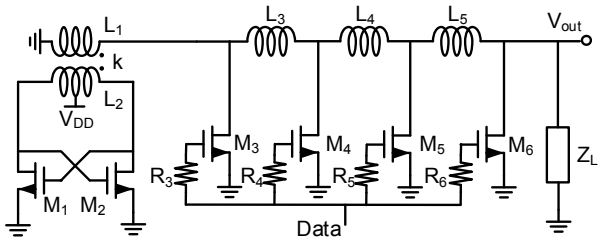

Fig. 4. Schematic of the transmitter, including a transformer based signal generator, and a SPST switch based OOK modulator.

For high-speed communication, a passive cascaded SPST switch based OOK modulator is designed to minimize the insertion loss with a high on-off ratio. When the input data is "0", The OFF-state transistors are represented as parasitic capacitors to cooperate with the series inductors for the signal transmission. When the input data is "1", the ON-state transistors are represented as small resistors to bypass the signal to ground. The more stages of transistors, the better on-off ratio but the larger insertion loss. With the tradeoff of the insertion loss and the on-off ratio, the aspect ratio of (W/L) = 24.48 µm / 0.065 µm (C_{off} = 20 fF and R_{on} = 15 Ω) transistors are employed. The series inductor is implemented with a 66 µm long MSL.

Figure 5 depicts a full differential receiver. The LNA features 3-stage cascaded common source amplification as shown in Fig. 5(a). The inter-stage coupling is achieved by transformers, which also serve as the inter-stage impedance matching. To connect with the channel, an on-chip balun is used to convert the single-ended input to differential outputs. The simulated gain of the LNA is 11.2 dB with 21-GHz bandwidth and the simulated noise figure is 7.5 dB.

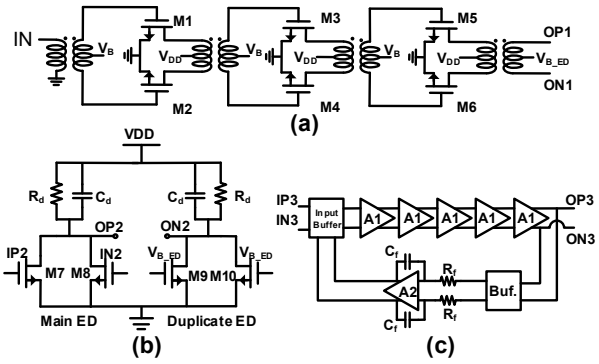

Fig. 5. Schematic of (a) the LNA, (b) the ED based demodulator, and (c) the LA based output buffer.

The ED, illustrated in Fig. 5(b), utilizes the square law feature of MOS transistors. The differential inputs are used to suppress the odd mode signals and realized by the output transformer of the LNA. To improve the common mode noise rejection, the duplicated ED is employed and the four inputs of ED are biased by the center tap of second coil of the ED input transformer. To maximize the responsivity, the ED is biased at class AB, that is, $V_B \approx V_{TH}$. The low pass filter (LPF) formed by C_d and R_d is used to filter the carrier and the higher order harmonics.

To further amplify the output voltage of the ED, a 5-stage common source (CS) LA with DC offset cancellation (DCOC) circuit is employed as shown in Fig. 5(c). The DCOC is integrator based LPF with R_f = 8 MΩ and C_f =10 pF with the about 2-kHz DC-offset corner. The simulated gain is 34 dB with 5 GHz bandwidth.

III. Experimental Demonstration

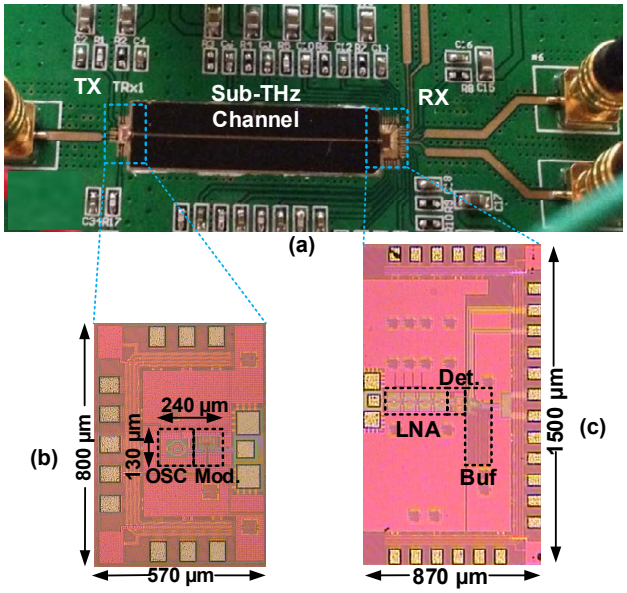

Fig. 6. (a) Test board of the sub-THz interconnect. (b) Die photo of the transmitter. (c) Die photo of the receiver.

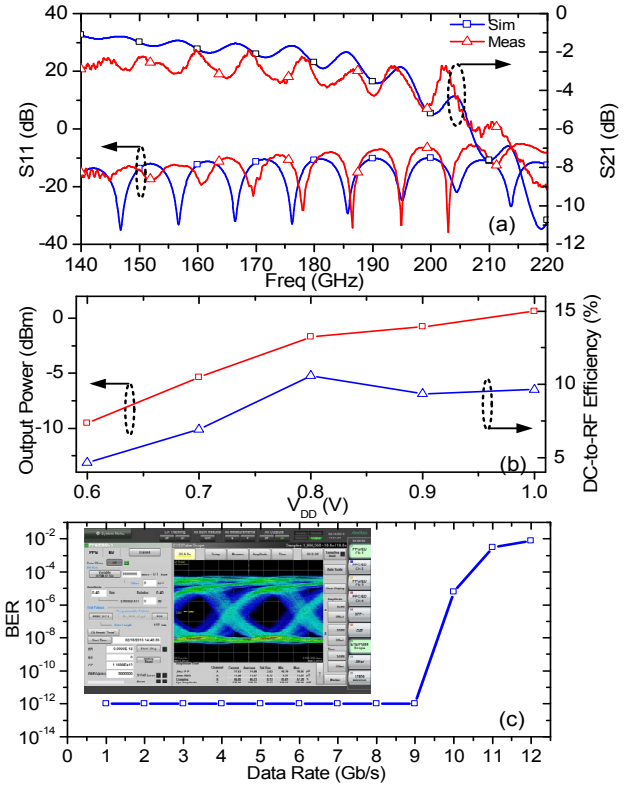

Fig. 7. (a) Measured S parameters of the channel. (b) Measured output power and DC-to-RF efficiency of the transmitter. (c) BER versus data rate with an inset of the eye diagram at PRBS 2^7-1, 9 Gb/s and BER < $1e^{-12}$.

The MSL based sub-THz channel is fabricated on a 100-µm thick quartz substrate. The seed layers of 20/100 nm thickness Ti/Au (σ = 4.1x10^7 S/m) is deposited followed by the lithography and 2-µm gold electroplating. After photoresist removing, the thin layer is etched to form the channel pattern. Finally, the backside is metallized followed by the wafer dicing to define the channel boundary.

Figure 6(a) shows the test board of the sub-THz interconnect. First, the quartz substrate with the MSL is attached between the transmitter and receiver by the silver epoxy. Then, GSG pads of chips are bonded to those of the quartz by gold wires. The transmitter and receiver chips are implemented in a 65nm bulk CMOS technology and die photos are shown in Fig. 6(b) and (c). The chip areas of transmitter and receiver are 570 µm × 800 µm and 870 µm × 1500 µm, respectively.

The measured insertion loss of the channel with the length *l* = 8.1 mm is 2 dB at 160 GHz with a 3 dB bandwidth of larger than 65 GHz as shown in Fig. 7(a). The measured output power and DC-to-RF efficiency with the various power supply at 165 GHz are shown in Fig. 7(b). The maximal output power is 0.63 dBm with 1-V power supply and 12 mA DC current. The best efficiency is 10.6% with 0.8 V. The measured bit-error rate (BER) versus data rate with an inset of the eye diagram is drawn in Fig. 7(c). The 2^7-1 PRBS pattern is generated from Anritsu MP2011B. The data rate is up to 9 Gb/s for a 22.6 mm MSL. The power consumptions of the transmitter and the receiver are 8.8 mW and 60.8 mW, respectively. Table I compares this work with other state-of-the-art interconnects.

TABLE I Comparison with the state-of-the-art interconnects

	JSSC 2013[2]	ISSCC 2015[4]	IMS 2015[3]	This work
Electrical / Optical	E	O	E	E
Technology	40nm CMOS	28nm SOI CMOS	65nm CMOS	65nm CMOS
fc	135GHz	194THz	85GHz	165GHz
Modulation	OOK	OOK	OOK	OOK
Data Rate (Gb/s)	10	25	NA	9
Power (mW)	98	123	13	69.6
Channel	Wireless	Wireline	Wireline	Wireline
Distance (mm)	100	N/A	2.5	22.6
Channel Loss (dB)	N/A	N/A	25	4@ 165GHz
Chip Area (mm^2)	2	N/A	0.42	1.76
Energy Eff (pJ/b)	9.8	4.9	NA	7.7

IV. Conclusion

This paper presents the design and the demonstration of the microstrip line based sub-THz interconnect for high energy-efficiency chip-to-chip communication. The low-loss passive channel and low-power transceiver chips are employed to boost the energy efficiency to 7.7 pJ/b. This technique can be readily scaled up to THz frequencies.

Acknowledgement

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