Low-loss and Broadband G-Band Dielectric Interconnect for Chip-to-Chip Communication

Bo Yu, Yuhao Liu, Yu Ye, Xiaoguang "Leo" Liu, and Qun Jane Gu

***Abstract*—This paper presents a novel dielectric waveguide based G-band interconnect. By using a new transition of microstrip line to dielectric waveguide, the interconnect achieves low insertion loss and wide bandwidth. The measured minimum insertion loss is 4.9 dB with 9.7 GHz 1-dB bandwidth. Besides, the structure is based on standard micromachined processing and easy to integrate with conventional packaging.**

***Index Terms*—Deep reactive ion etching, dielectric waveguide, G-band, interconnect, micromachined, sub-THz, transition.**

I. Introduction

FUELED by the demand of high data rate and low loss chip-to-chip communication, the interconnect gap have been a challenging issue over decades [1], [2]. Sub-THz/THz interconnect, using the spectrum sandwiched between optical and microwave frequencies, holds high potentials to fill the interconnect gap with wide bandwidth density and high energy efficiency by leveraging advantages of both optical and electrical interconnect approaches: low loss quasi-optical channels as well as advanced high speed semiconductor devices [3].

In general, the interconnect can be classified into three types, transmission line, including microstrip line (MSL), coplanar waveguide (CPW), grounded CPW, etc., metallic waveguides (MWG), and dielectric waveguide (DWG). The key aspects for inter-chip interconnect include low loss, wide bandwidth, reliable and compatible fabrication with silicon processes. The DWGs with low loss dielectric material have much less losses than transmission lines and MWGs since the conduction loss is avoided [4]–[7]. The loss for the CMOS transmission line is about 1 dB/mm at 100 GHz and 2 dB/mm at 150 GHz and increases fast with frequency [8], [9]. Moreover, from the process-compatible point of view, the DWGs are easier to fabricate and potentially compatible with integrated silicon circuits compared with MWGs. The comparison table is listed in Table I.

In this work, we propose a G-band (140-220 GHz) interconnect by combining the MSL and DWG. Compared with other interconnect, the proposed interconnect is low loss, wide bandwidth, fully micromachined, and easy to integrate with conventional packaging. The channel design methodology can be readily applied to higher frequencies in the THz range.

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TABLE I
COMPARISON AMONG DIFFERENT TECHNOLOGIES OF INTERCONNECTS

Design	Type	Loss (dB/mm)	Planar Process Integration
[5]	DWG	0.058 @ 500 GHz	Hard
[6]	MWG	0.05 @ 105 GHz	Hard
[7]	MWG	0.15 @ 600 GHz	Hard
[8]	MSL	2 @ 150 GHz	Easy
This work	DWG*	0.014 @ 140-190 GHz	Easy

*Without the transition

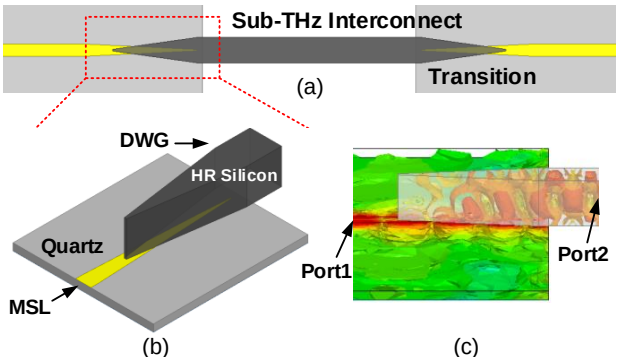

Fig. 1. (a) Top view of the G-band interconnect, (b) perspective view of the transition, (c) the magnitude of E-field distribution of the transition at 160 GHz.

II. Interconnect Design

Fig. 1(a) and (b) shows the configuration of the proposed G-band interconnect channel with two back-to-back transitions between the DWG and the MSL. Each transition consists of a tapered DWG and MSL to transit the electromagnetic wave smoothly. These two tapers overlap each other without gap. The 50-Ω MSL is designed on a 100-μm quartz substrate with the metal width of 218 μm. The straight DWG with 450-μm width and 500-μm height is designed according to [3]. The magnitude of E-field distribution of the transition is plotted in Fig. 1(c), which indicates the smooth mode transition between the MSL and the DWG.

The cross-section of simulated E-field distributions for the transition are illustrated in Fig. 2. The mode gradually transitions from the quasi-TEM in the MSL as shown in Fig. 2(b), to the hybrid mode in transition as shown in Fig. 2(c) and (d), and then to the E_{y11} mode in the DWG as shown in Fig. 2(e). The essential part of the transition design is the impedance matching. The characteristic impedance of the DWG and the MSL are plotted in Fig. 3. The real part of the characteristic impedance for the MSL decreases monotonically with the increase of the metal width. It is 50 Ω with the 218-μm width

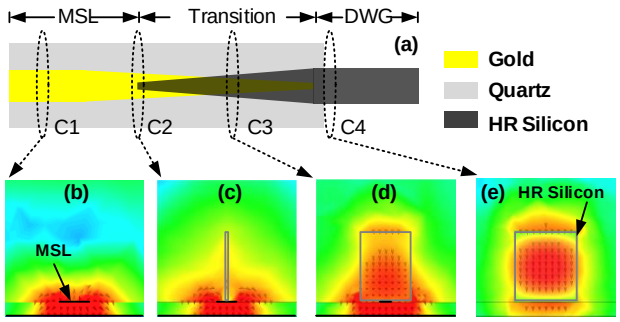

Fig. 2. (a) MSL to DWG transition structure, cross-section views of the E-field distribution at (b) C1, (c) C2, (d) C3, and (e) C4 depicted by HFSS.

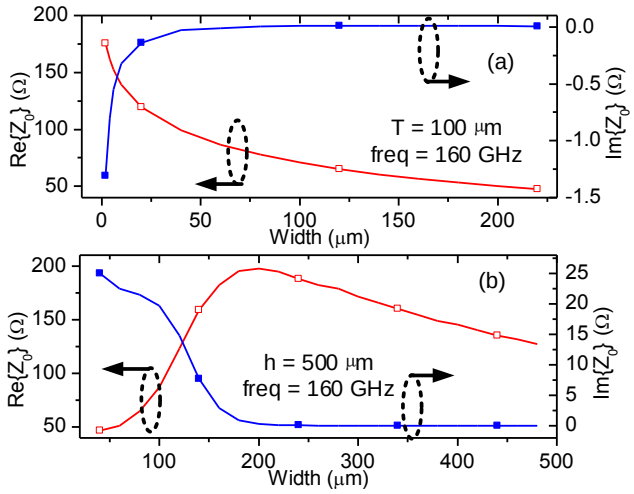

Fig. 3. Simulated characteristic impedance of (a) the MSL, and (b) the DWG. The thickness T of the quartz substrate is 100 μm, and the thickness h of the high resistivity silicon is 500 μm.

and 120 Ω with the 20-μm width. For the DWG, the real part of the impedance increases and then decreases with the increase of the DWG width because the dominant mode is changed from the evanescent mode to the E_{y11}. It is 45 Ω when the DWG width is 30 μm and 133 Ω when the DWG width is 450 μm.

To describe the matching performance, the theory of small reflections is used to analyze the reflection coefficient response as a function of the impedance taper versus position [10]. The incremental reflection coefficient from impedance step at x axis is given by

$$\Delta\Gamma = \frac{(Z+\Delta Z)-Z}{(Z+\Delta Z)+Z} \simeq \frac{\Delta Z}{2Z} \tag{1}$$

where Z is characteristic impedance, ΔZ is the impedance change step. Therefore, the total reflection coefficient is derived as

$$\Gamma(2\beta l) = \frac{1}{2}\int_{x=0}^{l} [e^{-j2\beta x}\frac{d}{dx}\ln(\frac{Z(x)}{Z(x=0)})]dx \tag{2}$$

where x is the taper position, l is the taper length, and β is the propagation constant. According to (2), the reflection coefficient of the transition with the various taper length is calculated compared with the simulated results in Fig. 4. The

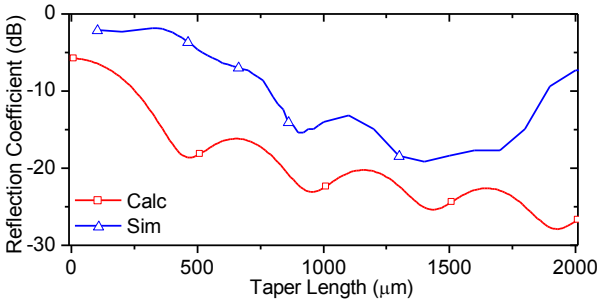

Fig. 4. Calculated and simulated the reflection coefficient of the transition with the various taper length at 160 GHz.

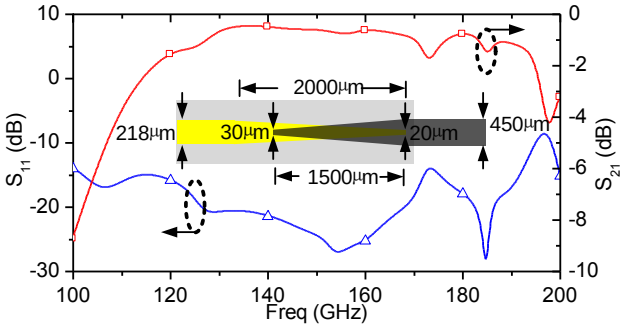

Fig. 5. Simulated S-Parameters of the transition. Dimensions of the transition are labeled in the schematic inside.

difference between the calculation and the simulation is due to the slight impedance mismatch between the MSL and the DWG at 160 GHz. As shown in Fig. 4, the optimized taper length is about 1500 μm. The minimum insertion loss for the transition is 0.44 dB with 51.9-GHz 1-dB bandwidth as shown in Fig. 5.

The complete interconnect consists of a 10-mm straight DWG with two back-to-back transitions in Fig. 6. Fig. 6(a) shows an interconnect with a separate substrate, and Fig. 6(b) shows the one with a joined substrate and backside metal. The minimum insertion loss is 1.55 dB with 38.9 GHz 1-dB bandwidth for the separate substrate and is 0.96 dB with 42.5 GHz 1-dB bandwidth for the joined substrate as shown in Fig. 6(c). To simplify the fabrication processing, the design presented in this paper chooses the joined substrate.

III. Experimental And Discussion

The fabrication processes of the interconnect with fabricated photos are summarized in Fig. 7. A 500-μm thick high resistivity (HR) silicon wafer (ρ = 10000 Ω · cm, ε_r = 11.9, tanδ = 0.001) is first patterned with a thick (∼ 12 μm) photoresist (AZ9260) to define the waveguide geometries. Then, the HR silicon wafer is attached to a carrier substrate and etched through in a DRIE process. The coupling structure is fabricated on a 100-μm quartz substrate (ε_r = 3.78). The coupling structure is patterned with a Ti/Au (σ = 4.1×10^7 S/m) thin film of thickness 20/200 nm by a lift-off process. Both DWG and MSL photos are shown in Fig. 7.

The measurement setup consists of an Agilent network analyzer (PNA-X N5247A), a pair of Virginia Diodes fre-

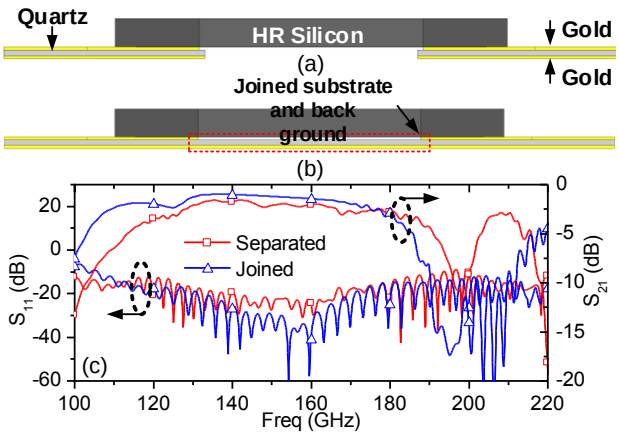

Fig. 6. (a) Side view of the interconnect with a separate substrate, (b) side view of the interconnect with a joined substrate and back ground, and (c) simulated S-parameters for both structures.

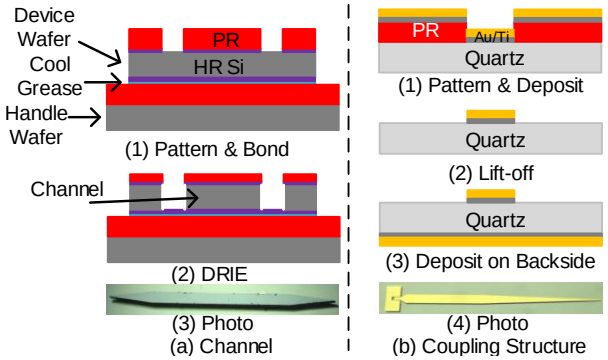

Fig. 7. Fabrication procedure and the photos of (a) the DWG, and (b) the coupling structure.

quency extension modules (VDI WR5.1-VNAX), WR-5 (140-220 GHz) S-bend waveguides, and a pair of WR-5 probes. The SOLT (Short, Open, Load, Thru) calibration method is employed to set the reference plane at the probe tip. Therefore, the measured interconnect path includes the interconnect, two 1.4-mm MSLs, and two CPW-to-MSL transitions. The alignment is completed by using alignment marks on the each side of coupling structure of designed on the quartz substrate.

Fig. 8 presents the simulated and measured S-parameters of the interconnect. The measured minimum insertion loss for the 10-mm interconnect is 4.9 dB with 9.7-GHz 1-dB bandwidth, and the simulated one is 1.6 dB as shown in Fig. 8. The 3.3-dB discrepancy between the measurement and the simulation may come from the air-gap between the MSL and the DWG, material characterisitics, limited fabrication resolution, and calibration inaccuracy. Besides, Fig. 8 shows the comparison for the DWG with two different lengths: 10 mm and 20 mm. These two interconnects have very close insertion loss performance, which indicates that DWG channel loss is very small and the major loss comes from the transitions. By taking the average difference from 140 to 190 GHz, the attenuation constant is about 0.014 dB/mm indicated in Table I.

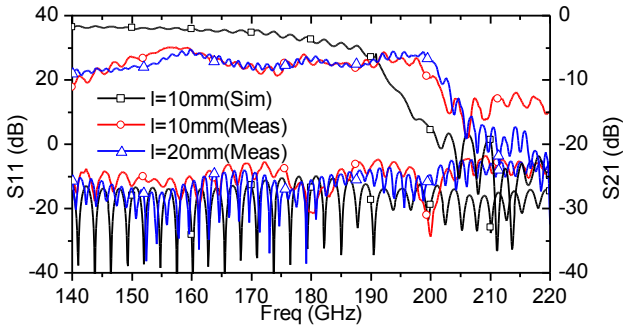

Fig. 8. Comparisons of the simulated and measured S-parameters for a 10-mm and 20-mm length l channel.

IV. Conclusion

In this paper, a low loss and wide bandwidth G-band interconnect is presented, which is compatible with planar integrated circuits (ICs) process. A prototype has been designed, fabricated and measured to validate the proposed scheme. The measured minimum insertion loss is 4.9 dB with 9.7-GHz 1-dB bandwidth. The results can be further improved by reducing the gap and the assembly offsets between the MSL and DWG. This new interconnect is based on standard micromachined processing method, making it compatible with standard packaging method. Besides, it can be easily extendable to THz frequencies due to the low insertion loss and no conduction loss with HR silicon DWG.

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