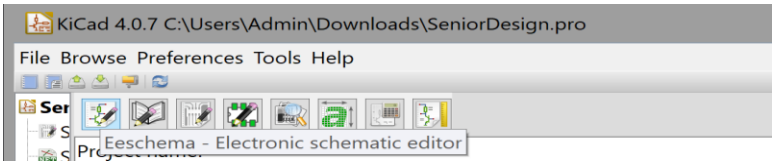
ABSTRACT

This tutorial will give a general walk-through of how to create a PCB and some of the issues that may arise during the process. The first and most important thing to remember is to read/watch all of Professor Liu's supplementary material including the Blinky tutorials. It allows you to become familiar with KiCad's nuances, which will allow you to save a lot of time once you begin your design.

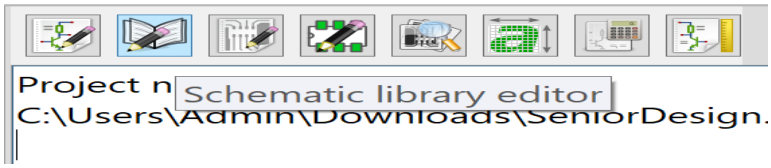
THE DESIGN

SCHEMATIC & SCHEMATIC LIBRARY EDITOR

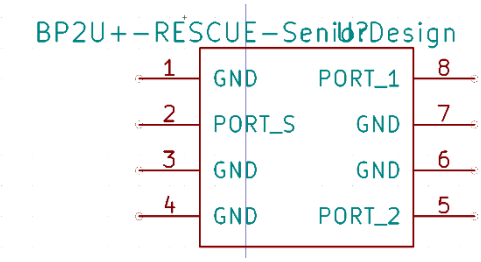
Leading up to the PCB you need to ensure that you first have a working schematic. This is done by using KiCad's schematic editor. The symbol to reach this is shown below with the symbol highlighted in blue.



Most of the components can be found in the device library such as resistors, capacitors, potentiometers etc. Utilizing the default libraries now will make association in the netlist much easier later. However, if the component isn't available then you will need to use the schematic library editor. In general, it is a good idea to include plenty of test points in your design after critical functionality for debugging if, and most likely when, the system doesn't behave as intended. To symbol to reach the library editor is shown below, highlighted in blue.

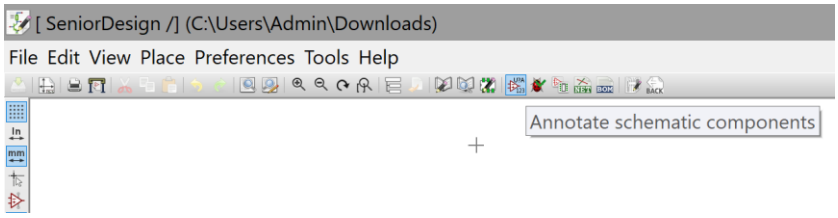


In order to create your own component use the preference tab in the schematic library editor to select the datapath to the library. The folder for the new library will need to be in the same directory as the .pro file. Select the icon to create a new component. Remember to label the component as the part number to make the design easier to read. Also, the pins must be labeled as this will be matched to the datasheet in the footprint section. Once the component is saved in the library it can be accessed in the schematic editor. Below, is an example of a custom layout for our power splitter.

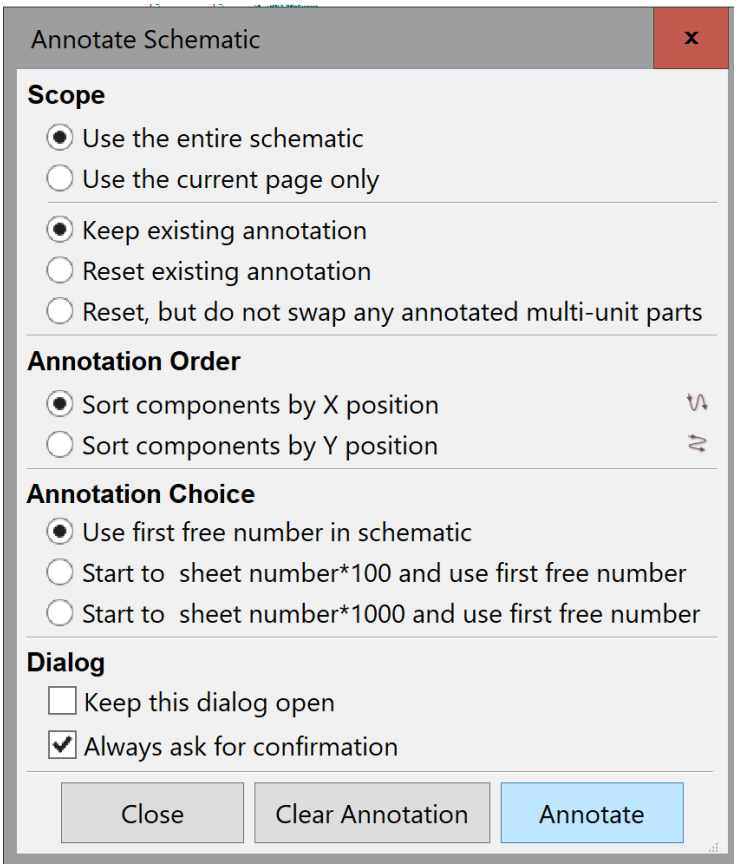


When arranging the schematic, it is good practice to keep components and its biasing circuits in a modular form so when proofreading it will be less time consuming when all functions are clear and separated. An important step here is to make sure that all components include a biasing circuit (if provided in the datasheet) as well as ensuring that the bias is for the correct frequency, otherwise, the design will not perform as expected.

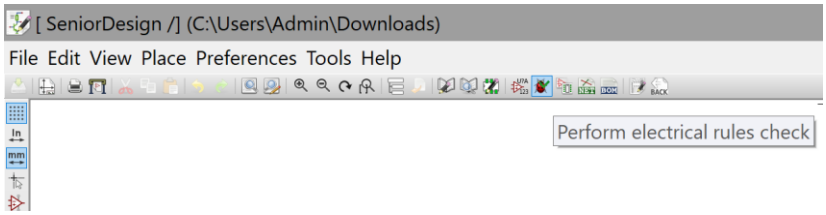
Once the main design is completed run an annotation, which will label components from left to right. The annotation is accessed from the schematic window shown below.



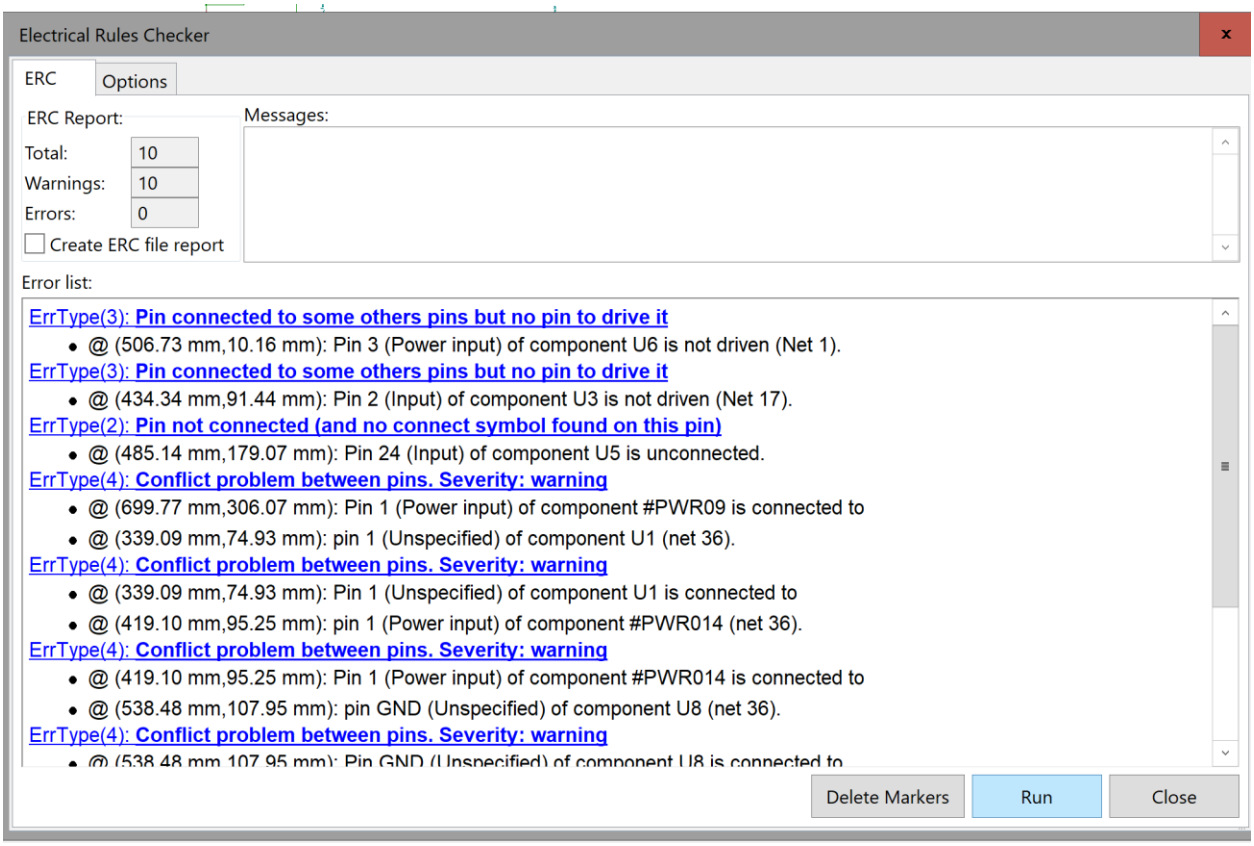
This will create a pop-up window as shown below. Click annotate and the components will automatically be labeled.



Next, run an electrical test. This will make sure all wires are connected and no rules are violated. Keep in mind this doesn't mean that there aren't any errors in the functionality of the design. The electrical test symbol is also in the schematic window and shown below.



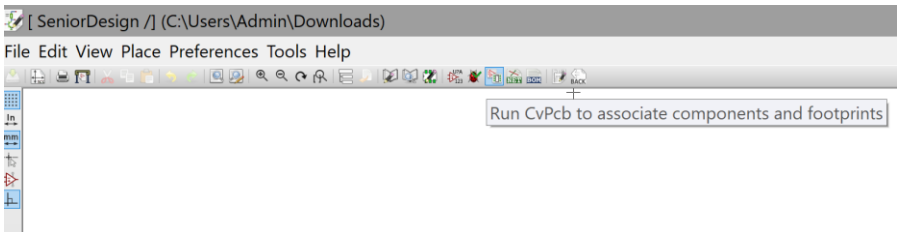
An example of an electrical test output is shown below. Most errors are just warnings and can be ignored.



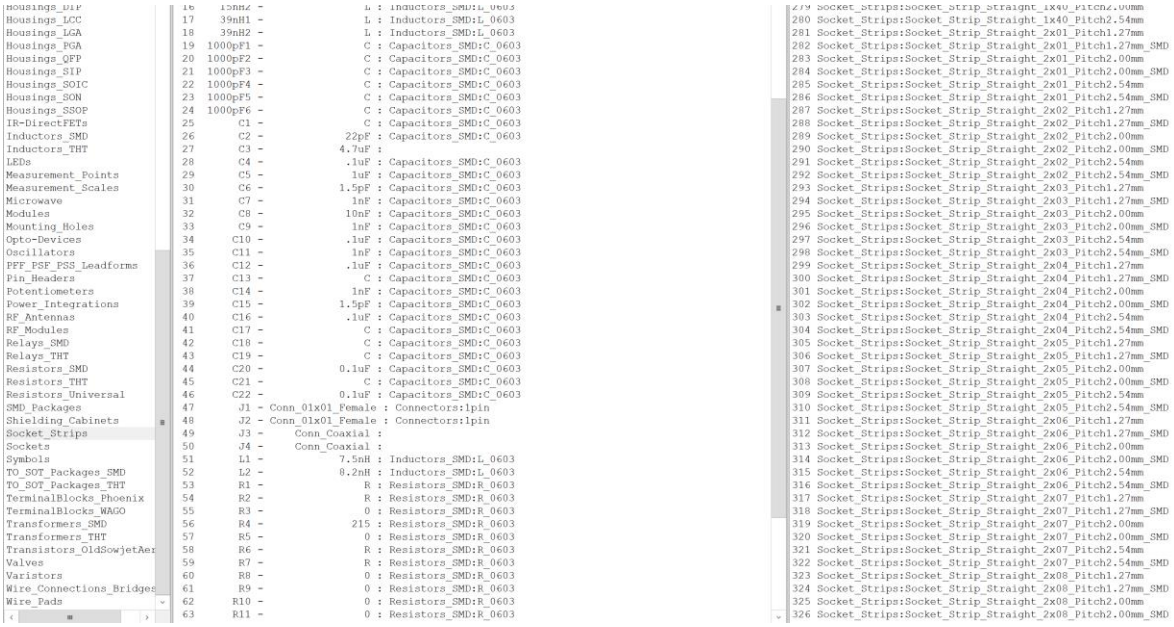
As a suggestion make sure that everything on the schematic is reviewed by all team members and someone from a different group or TA. This is the easiest place to correct errors because all following steps will depend on what is present in the schematic. If you want to change anything later, you will need to edit the schematic and update the netlist and PCB.

NETLIST & FOOTPRINT EDITOR

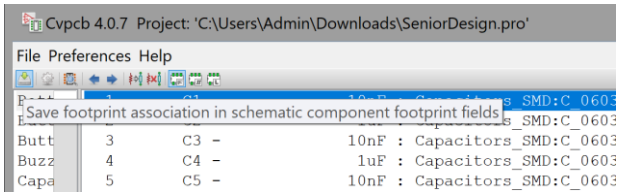
After careful evaluation of the schematic and it is determined there is no error in the design go to the KiCad symbol in the schematic window and click on run CvPcb to associate component as shown below.

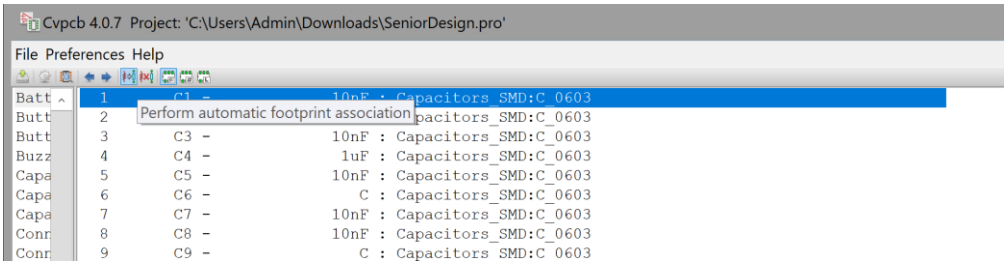


This will take you to the association of components called the netlist.

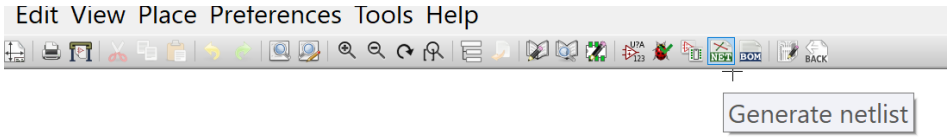


For this part all passive component will be using the SMD 0603 and the active components will vary with through hole and SMD. An example of the netlist component selection is shown above.If you can, choose components that are SMD because it will allow for less interference as well as be easier to use with multi-layer designs (quarter two). For the most part, the common components will be available in the libraries provided. Otherwise, you will need to create a customized footprint, which will be discussed later in this tutorial. For the components that are included click on the save footprint associate link symbol and automatic footprint association shown in the two figures below.

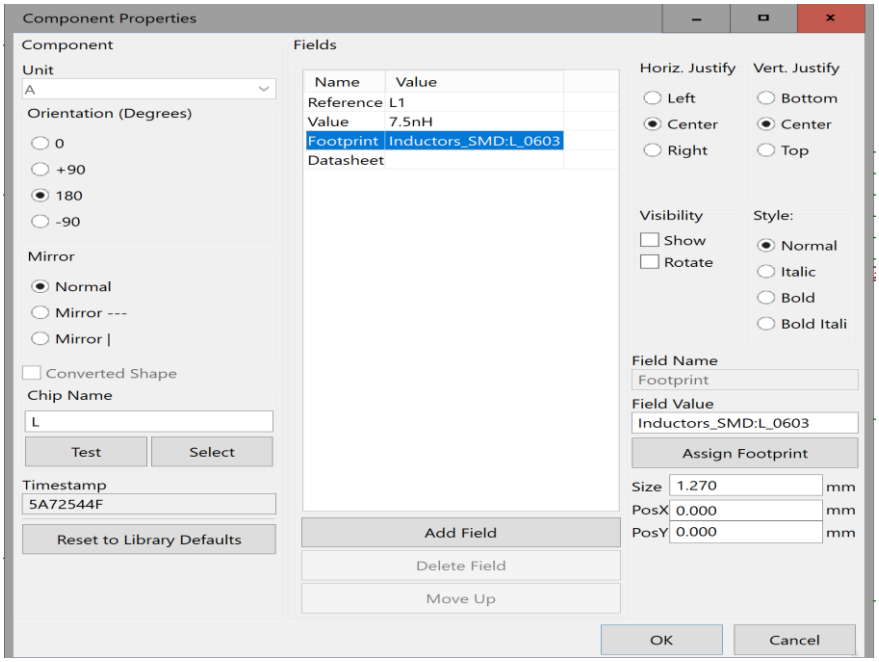




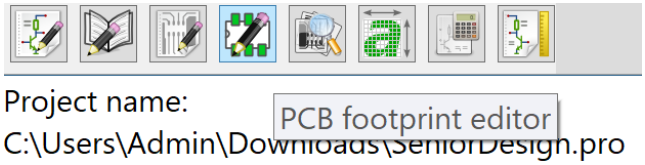
To make sure that the footprints have been saved go back to the schematic editor and click on the generate netlist symbol shown below.



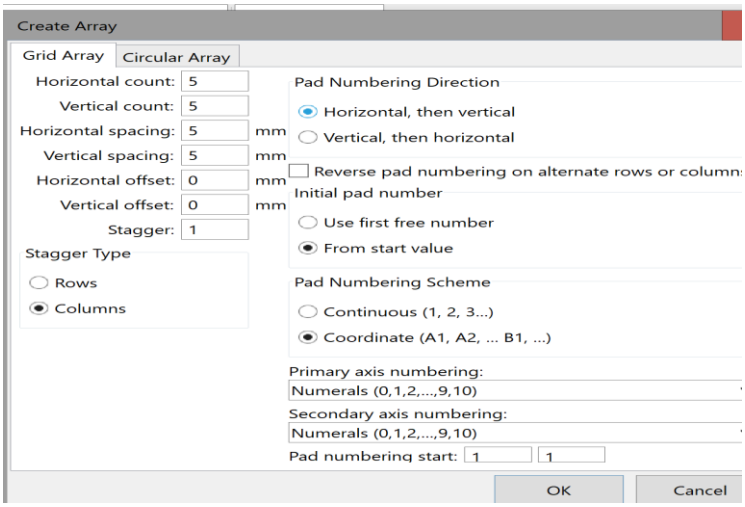
If the association has worked then clicking on the component properties in the schematic will now show the associated footprint. An example of what this should look like is below.



If your component is unique and requires a custom footprint you will need to perform similar steps as the schematic component editor. To open the footprint editor click on the symbol from the main windown as shown below.



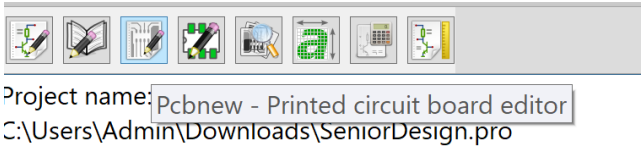
Make sure to meticulously go over the datasheet to make sure the measurements are correct. Check to see if values are reported in mils or mms. If there are multiple pads then KiCad has a create pad array option.This allows you to set an accurate spacing between pads. To access this option, you must first lay a pad down and then right click. Click on create pad array and a pop-up window like the one shown below should appear.



Make sure to check the datasheet to see if the component package is SMD or through hold and make that selection. Again save this component in the same directory (it should be .pretty format). You will now be able to place the component in the PCB editor.

PCB

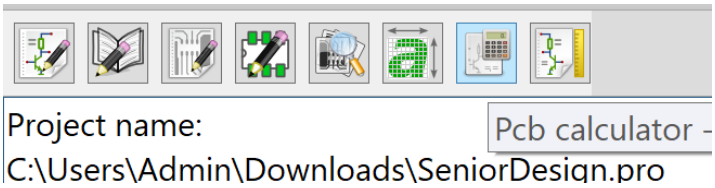
The PCB window is accessed by clicking on the PCB symbol as shown below, highlighted in blue.



This will pop up a blank window in which you will need to click on the generate netlist again. This will connect the footprints with the schematic components. All of the components will originally be placed on top of each other, so you will need to right click to spread them out. You will notice the pin

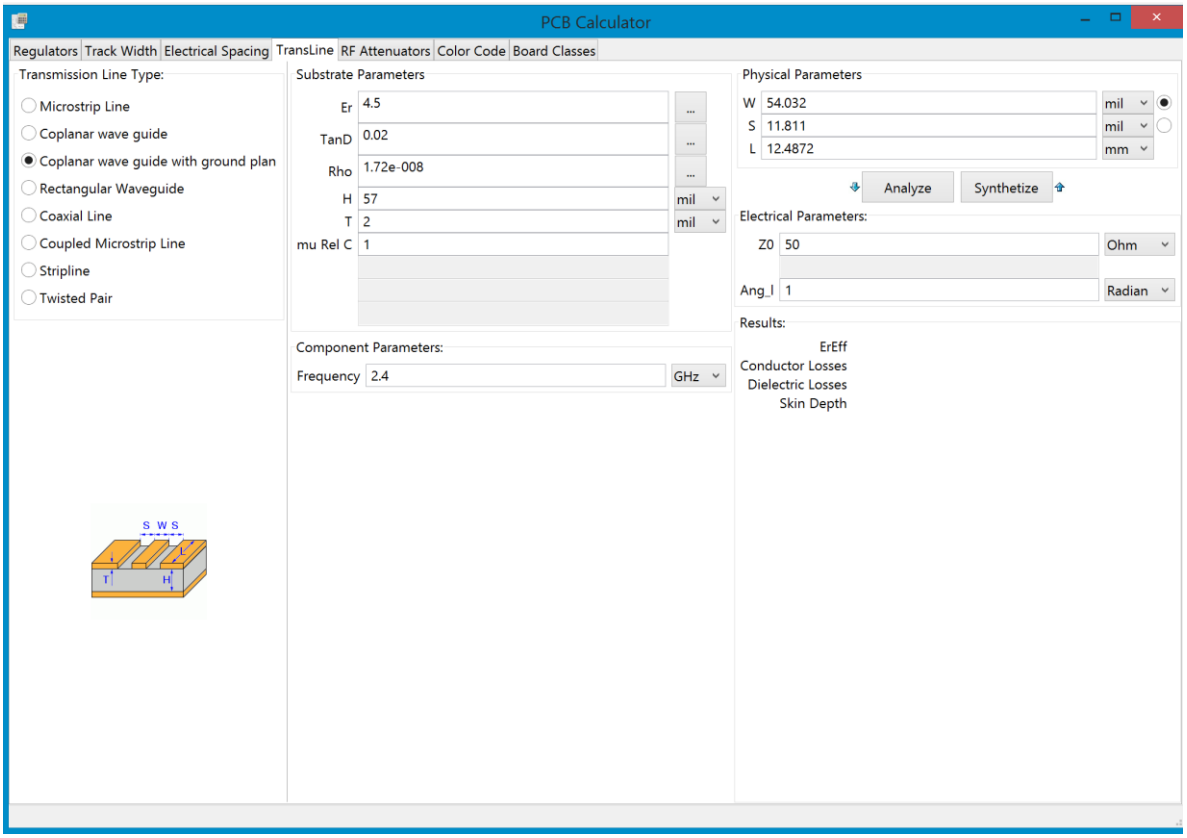
connections from the schematic are shown in the PCB as wires connecting. This is why it is critical to complete all edits and update the schematic or else it won't be updated in the final PCB product.

Since we are using RF components we will need to have impedance matching in our traces. This can be completed by using KiCad's PCB calculator, which can be found on the original screen as shown below.



The PCB should begin with edge cuts. In quarter 1 these dimensions are given so start with these outlines. For quarter 2, since the size will be measured it is best to have as compact a system as possible without forfeiting functionality. These edge cuts will also be required for DFM reports.

For our design, we will be using a coplanar waveguide with a ground plane. As shown below, you will



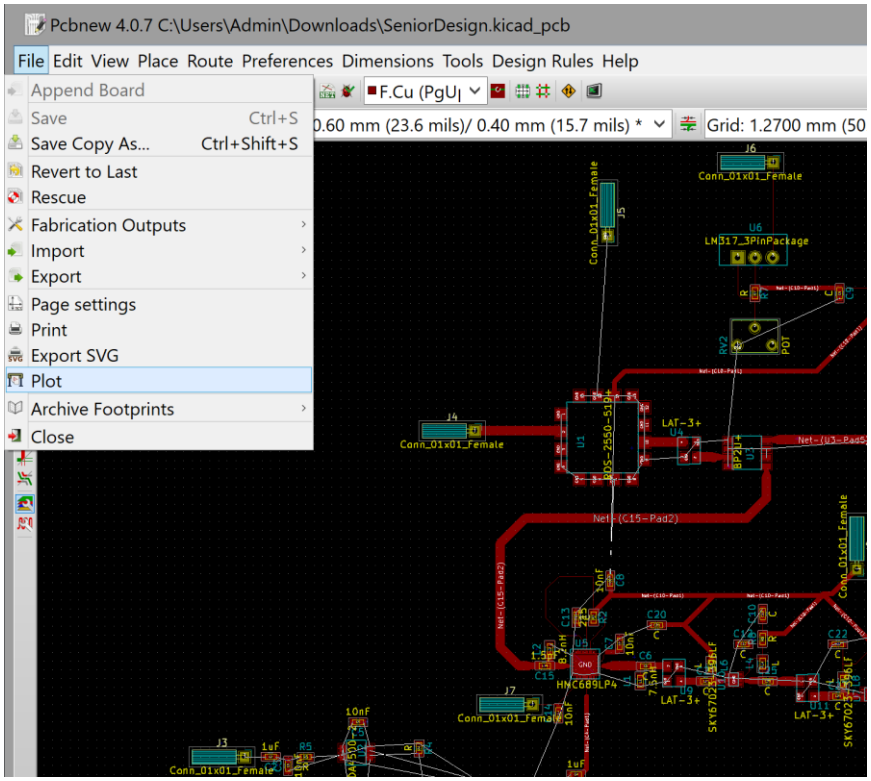
need to choose the thickness of the board which has limited values based on manufactures specs. We used 0.62 in. The dielectric spacing is given by the dielectric being used. This is also the value that must be used in the spacing when you do a ground fill. With length we can use 1 as this will not change the width calculation significantly. After these values are typed in we changed the width until we have outputted a value close to 50 ohms. This is the width of the trace you must use.

A good habit for RF components will be to keep them as close and straight as possible. This will allow the signal to avoid as much power consumption as well as limit interference. Having curved traces will create opportunity for more reflection in the system. After RF traces have been placed the other components only need a large enough trace for power to pass through.

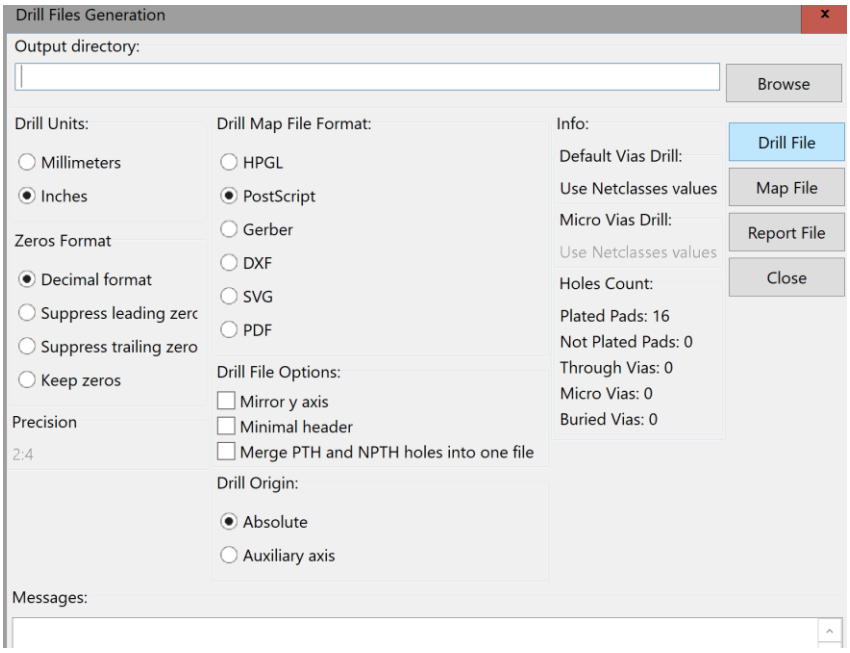
Once all traces have been placed and all connections connected, a ground plane will be placed as well. Remember the spacing in the PCB calculator will be the spacing between the trace and plane. This will allow for less interference. If a ground plane is laid and any changes occur, make sure to replace the ground plane. Now vias should be placed to stich the top and bottom of the board together. Vias should especially be placed near RF traces and components to reduce the interference.

DFM REPORT

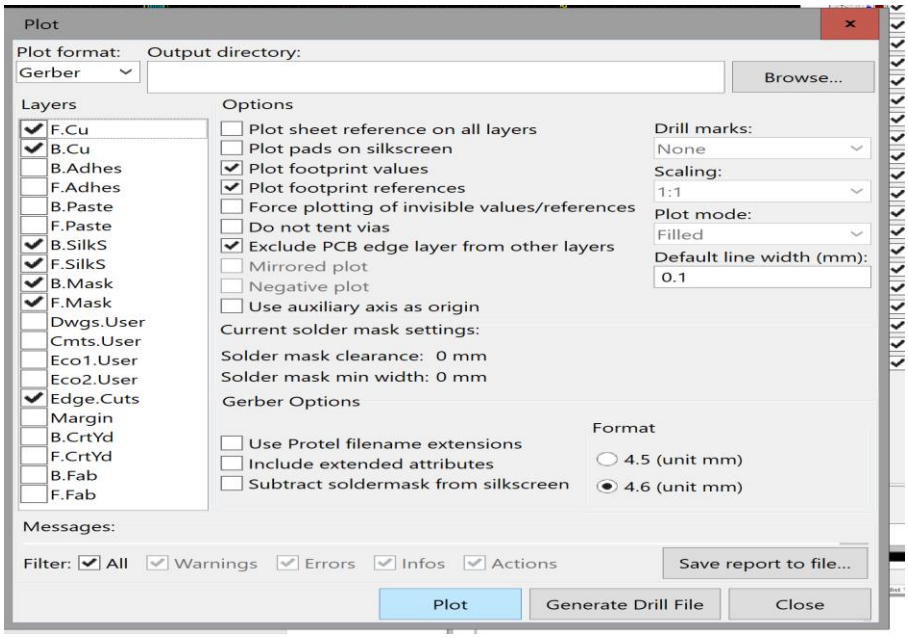
Once the design again has been checked multiple times by multiple people(It is good to use the checklist the professor offers) then it is ready to be checked for manufacturer issues NOT design issues. This is done by going to the plot tab in the PCB window shown below.



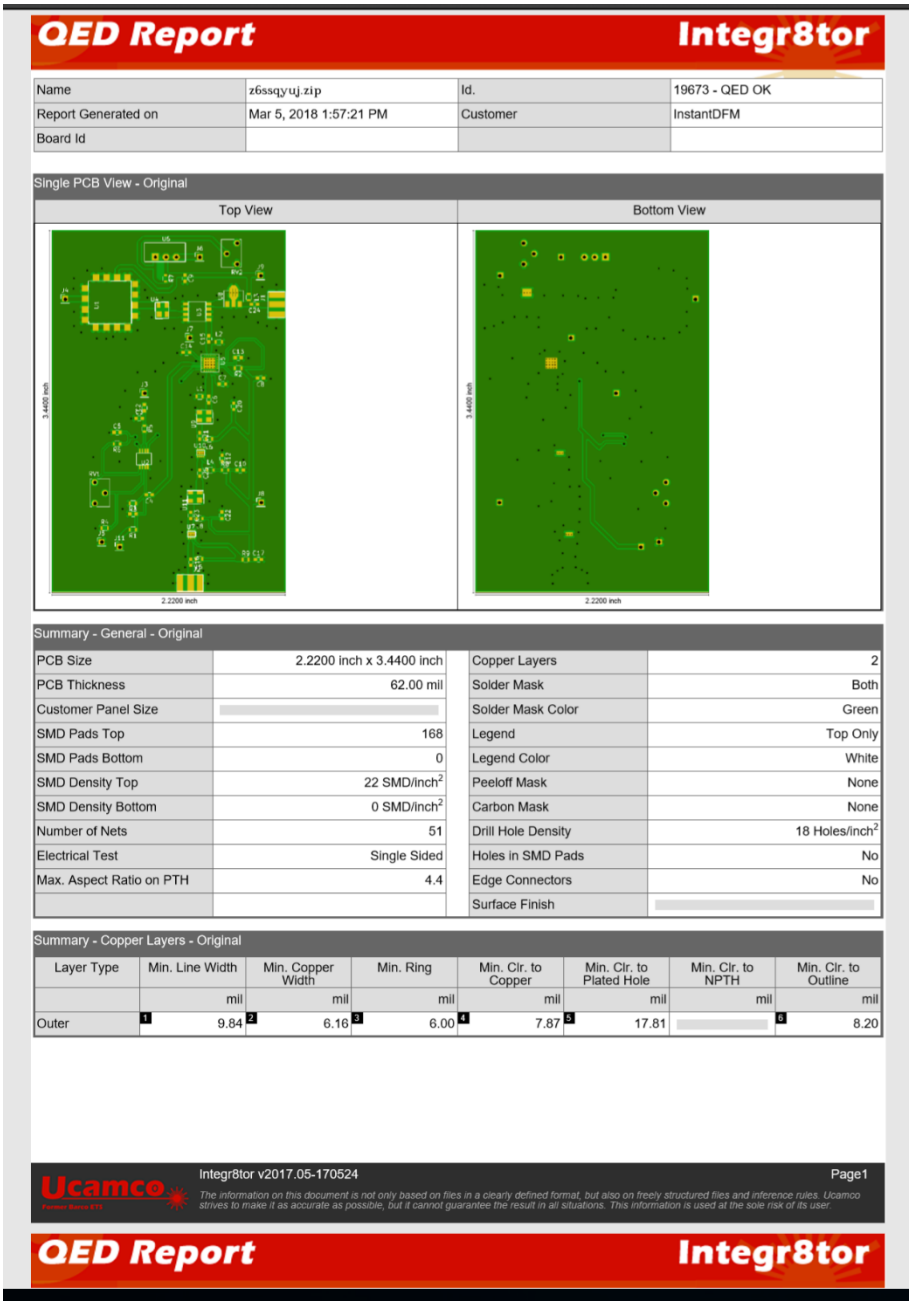
First the drill file will be created as shown below.



Then the layers that should be selected are shown in the figure below ZIP the plot and drill files and then submit on the Bay AREA Circuits DFM Report. The values that are flagged here are mostly for manufacturer capabilities. Make sure the capabilities you are considering are part of the student special limits. Even if there is no error there may still be a design issue.



The DFM report will look like the figure below. Check the summary values for warnings and errors, but also check the whole report for any red boxes as these will not be within capabilities.



QED Report — Integr8tor

Name	z6ssqyuj.zip	Id.	19673 - QED OK
Report Generated on	Mar 5, 2018 1:57:21 PM	Customer	InstantDFM
Board Id			

Single PCB View - Original

Top View | Bottom View

Summary - General - Original

PCB Size	2.2200 inch x 3.4400 inch	Copper Layers	2
PCB Thickness	62.00 mil	Solder Mask	Both
Customer Panel Size		Solder Mask Color	Green
SMD Pads Top	168	Legend	Top Only
SMD Pads Bottom	0	Legend Color	White
SMD Density Top	22 SMD/inch^2	Peeloff Mask	None
SMD Density Bottom	0 SMD/inch^2	Carbon Mask	None
Number of Nets	51	Drill Hole Density	18 Holes/inch^2
Electrical Test	Single Sided	Holes in SMD Pads	No
Max. Aspect Ratio on PTH	4.4	Edge Connectors	No
		Surface Finish	

Summary - Copper Layers - Original

Layer Type	Min. Line Width	Min. Copper Width	Min. Ring	Min. Clr. to Copper	Min. Clr. to Plated Hole	Min. Clr. to NPTH	Min. Clr. to Outline
	mil	mil	mil	mil	mil	mil	mil
Outer	1 9.84	2 6.16	3 6.00	4 7.87	5 17.81		6 8.20

Integr8tor v2017.05-170524 Page1

The information on this document is not only based on files in a clearly defined format, but also on freely structured files and inference rules. Ucamco strives to make it as accurate as possible, but it cannot guarantee the result in all situations. This information is used at the sole risk of its user.

QED Report — Integr8tor

SUGGESTIONS

- Don’t wait until last minute for Quarter 1 PCB Design. It seems like you have a lot of time, but there are a lot of small technical details to implement. Once the first PCB is due the next two will be due directly after and there will be little time to figure out issues.
- It is crucial to get a good review team. Even with multiple meticulous reviews something can always be found by another pair of eyes. Just make sure your review team will take the time to really review your PCB.
- Learning hotkeys will allow you to save a lot of time on designing and editing schematics.

- Review datasheets multiple times to make sure pads are the correct size and in the right measurement unit (mm or mil). Also, make sure the footprint pad numbers match the same pin numbers in the schematic.
- The SMA footprint provided is an aerial view of the connection and not the side view. Keep this in mind while selecting a footprint for the SMA in the netlist.
- Avoid using 90° T connections in the PCB
- Use plenty of vias.
- It may help to use a socket connector instead of to directly solder some of the more sensitive components, so they don't burn out. This also will input more interference into the system so weigh the options to decide what option is superior for your system.