EEC134 Final Report

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I. SYSTEM DESIGN

Our main priorities for our quarter 2 system design was to make our system more compact to decrease weight and improve the maximum range of our radar system while still maintaining a similar design to our quarter 1 system. Our initial quarter 2 design consisted of a stacked PCB with our baseband PCB on the bottom and RF PCB above it and pin headers to connect the power and grounds to each other. This design would not only make our system lighter, without the need for breadboards or RF blocks, but also more compact and mobile which was a main concern for our quarter 1 system. Another modification we made from our quarter 1 system was including 4 LNA's after our receive antenna which would amplify our signal by up to 57 dB and increase the range of our radar. Since the LNA's are cascaded, the noise contribution from each LNA after the first one will be suppressed by the preceding stages which is important as we cannot allow the amount of noise from the amplifiers to drown out our received signal. However, looking back at our design, 2 LNAs would have been sufficient. Since each LNA draws around 70 mA of current, the amount of total power consumed by our system was hurt mainly by the excess of LNA's.


Fig. 1.　　　Block diagram

Fig. 2.　　　Transmit Section ADISimRF

		Stage 1	Stage 2	Stage 3	Stage 4	Stage 5	Stage 6	Stage 7	Stage 8	Sta...
Transmit Toggle Tx/Rx		Temp Part	Atten	Temp Part	LNA	Device	Device	Device	Device	Device
		Temp Part	Temp Part	Temp Part	PartNumber	PartNumber	PartNumber	PartNumber	PartNumber	PartNum
Output Freq	(MHz)	2445	2445	2445	2445					
Zin	(Ohms)	50	50	50	50					
Zout	(Ohms)	50	50	50	50					
Power Gain	(dB)	0	-3.03	-3.28	19					
Voltage Gain	(dB)	0	3	-3.3	19					
OIP3	(dBm)	100	100	100	37.5					
OP1dB	(dBm)	90	90	90	24					
Pout	(dBm)	6	2.9	-0.3	18.6					
Pout Backoff	(dB)	84	87.1	90.4	5.4					
Peak Backoff	(dB)	84	87.1	90.4	5.4					
Noise Figure	(dB)	0	3	3.3	3.5					
Voltage	(V)	5	0	3.3	5					
Current	(mA)	45	0	0	118					

Input			Analysis								
Number of Stages	10		Output Power (rms)	10.65	dBm	Noise Figure	9.81	dB	OIP3	37.5	dBm
Input Power	5.96	dBm	Output Voltage (rms)	1.91	Vrms	Output NSD	-151.5	dBm/Hz	IIP3	24.8	dBm
Analysis Bandwidth	1	MHz	Output Voltage (pp)	5.41	Vpp	Output NSD	6	nV/rtHz	IMD3 ((Pout-3dB) per tone))	-43.7	dBc
PEP-to-RMS Ratio	0	dB	OP1dB	24	dBm	Output Noise Floor	-91.5	dBm	SFDR	85.9	dB
P1dB Backoff Warning	0	dB	IP1dB	12.3	dBm	SNR	110.1	dB	ACLR (est.)	-58	dB
Peak Backoff Warning	0	dB	Power Gain	12.69	dB				Pwr Consumption	0.81	W
			Voltage Gain	12.69	dB						

Fig. 3.　　　Receive section ADISimRF

		Stage 1	Stage 2	Stage 3	Stage 4	Stage 5	Stage 6	Stage 7	Stage 8	St...
Transmit Toggle Tx/Rx		LNA	LNA	LNA	LNA	Mixer (Tx)	Device	Device	Device	Device
		Temp Part	Temp Part	Temp Part	Temp Part	Temp Part	PartNumber	PartNumber	PartNumber	PartNum
Output Freq	(MHz)	2445	2445	2445	2445	2445				
Zin	(Ohms)	50	50	50	50	50				
Zout	(Ohms)	50	50	50	50	50				
Power Gain	(dB)	17.9	17.9	17.9	17.9	-5.6				
Voltage Gain	(dB)	17.9	17.9	17.9	17.9	-5.6				
OIP3	(dBm)	33.6	33.6	33.6	33.6	100				
OP1dB	(dBm)	19.1	19.1	19.1	19.1	90				
Pout	(dBm)	-76.1	-58.2	-40.3	-22.4	-28				
Pout Backoff	(dB)	95.2	77.3	59.4	41.5	118				
Peak Backoff	(dB)	95.2	77.3	59.4	41.5	118				
Noise Figure	(dB)	0.5	0.5	0.5	5	5.6				
Voltage	(V)	3	3	3	3	5				
Current	(mA)	60	60	60	60	1110				

Input			Analysis								
Number of Stages	10		Output Power (rms)	-28	dBm	Noise Figure	0.51	dB	OIP3	27.93	dBm
Input Power	-94	dBm	Output Voltage (rms)	8.9	mVrms	Output NSD	-107.5	dBm/Hz	IIP3	-38.1	dBm
Analysis Bandwidth	1	MHz	Output Voltage (pp)	25.15	mVpp	Output NSD	943.8	nV/rtHz	IMD3 ((Pout-3dB) per tone))	-117.9	dBc
PEP-to-RMS Ratio	0	dB	OP1dB	13.43	dBm	Output Noise Floor	-47.5	dBm	SFDR	50.2	dB
P1dB Backoff Warning	1	dB	IP1dB	-51.6	dBm	SNR	19.5	dB	ACLR (est.)	-19	dBc
Peak Backoff Warning	1	dB	Power Gain	66	dB				Pwr Consumption	6.27	W
			Voltage Gain	66	dB						

II. ADISIMRF

ADISimRF allowed us to accurately predict how the elements in a chain would interact with each other. It allowed the team to be able to determine whether some parts fit into the overall design and it let us know the expected power outputs after any element. In addition, ADISIM provided useful predictions for how linear our amplifiers would perform based on OIP3 and OP1dB specifications, how much noise would contribute to the system based on Noise Figure and SNR, and how much total power would be consumed by our system based on expected current draw from each component. Having this information while debugging the RF board was very helpful.

Baseband PCB:

Component	Part Name
Voltage Regulator	LM317 *(Digikey)*
Voltage Reference	LT1009CLPE3 *(Linear)*
DAC	MCP4921 *(Digikey)*
Very Low-Noise Op-amp	TL974IN *(Mouser)*

RF PCB:

Component	Part Name
VCO	ROS-2490 *(Mini-Circuits)*
Attenuator	GAT-4+ *(Mini-Circuits)*
Power Splitter	SCN-2-27 *(Mini-Circuits)*
Power Amp	YSF-272 *(Mini-Circuits)*
LNA	TAMP-272LN+ *(Mini-Circuits)*
Mixer	MACA-63H+ *(Mini-Circuits)*
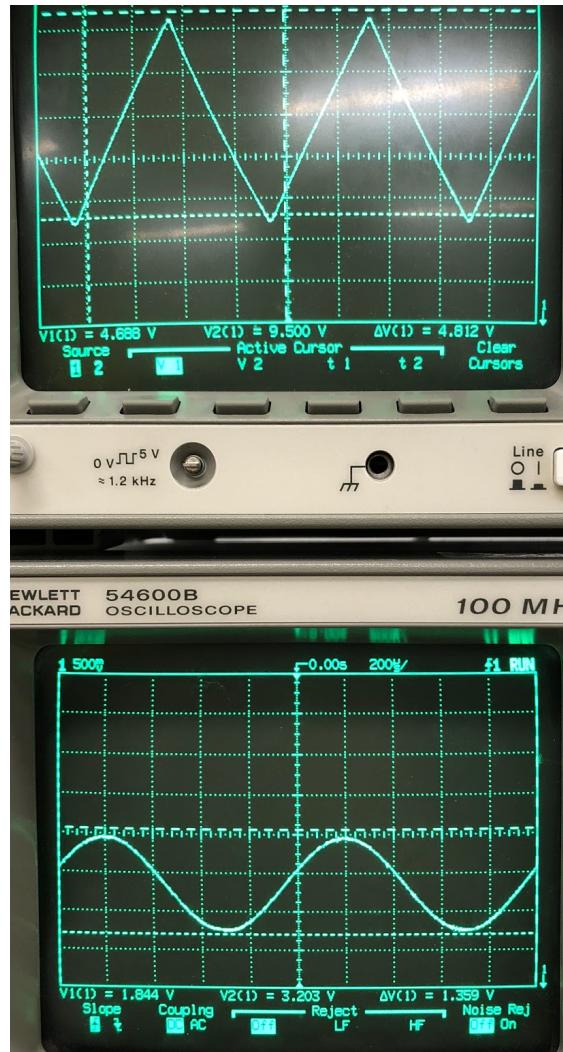
Fig. 4.   Top: DAC output with DC offset, Bottom: Baseband Amplifier output

Since the 5 Volt tuning VCO from our original Quarter 2 design was out of stock and not realized until after the PCB design was submitted, a new component was needed to replace the old VCO as well as additional circuitry to operate at the frequency range our system was built around. The best option available which had the same footprint as our original VCO was the ROS-2490+ VCO from Mini-circuits. Since this new VCO has a 10V tuning range, an additional DC offset circuit was designed to level shift our DAC output for a ~4.5-9.5V tuning range which corresponds to ~2.37-2.53 GHz output frequency range. This DC offset circuit consisted of a simple voltage divider and a large AC coupling capacitor.

III. PCB DESIGN

The PCB format was designed to have the baseband processing on one board, and to have the high frequency processing done on another board. The PCBs designed so that the high frequency board will sit on top of the baseband board, held by 4 #6 size screws. The two boards are connected with one another with Molex vertical 4 pin connectors, which we did not have a chance to crimp.

The baseband board used a LM317 to regulate the 8V input to 5V, and the LT1007 converted the 5V to a 2.5V output. The 5V rails were used to supply the RF PCB while the 2.5 rail was used to power the DAC and OP amp. The Teensy is used to output the sync which is sent to the transmit antenna. The Teensy also outputs the SDI and SCK signals to the DAC. The DAC output is a digital triangle wave. The gain stage and filter take in the IF output of the RF Board to filter out the higher frequency noise and to amplify the signal.
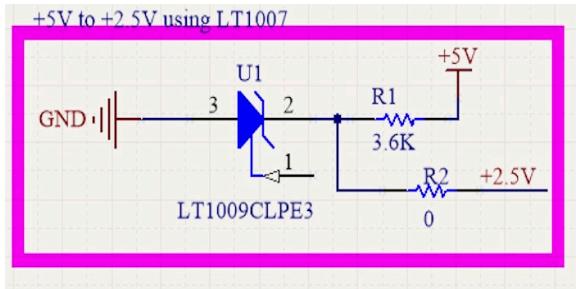
Fig. 5. Precision voltage reference
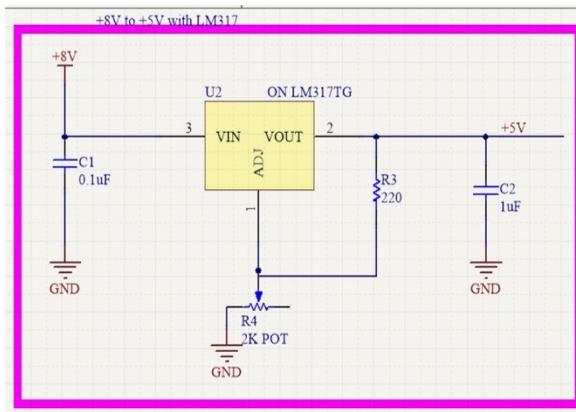
Fig. 6. Voltage regulation
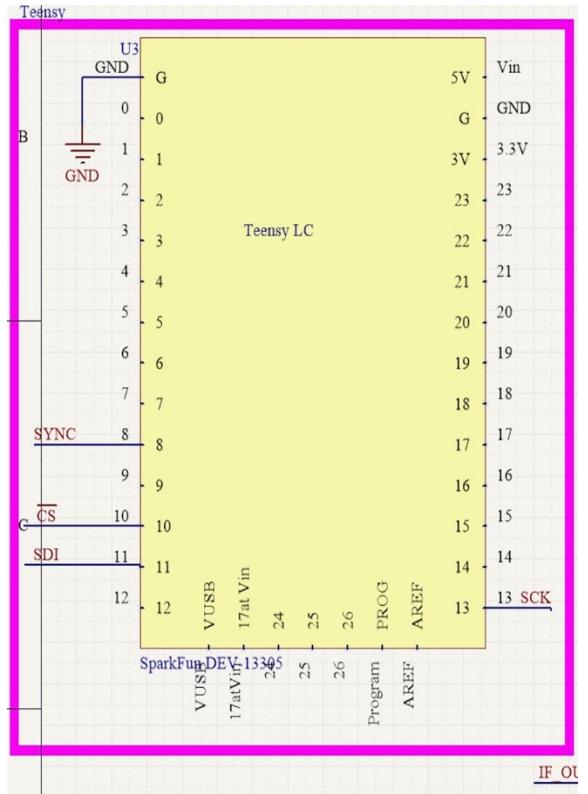
Fig. 7. Teensie schematic
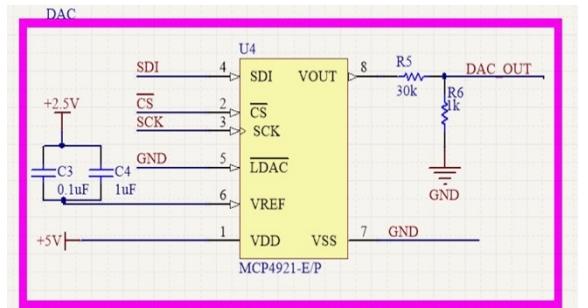
Fig. 8. DAC schematic
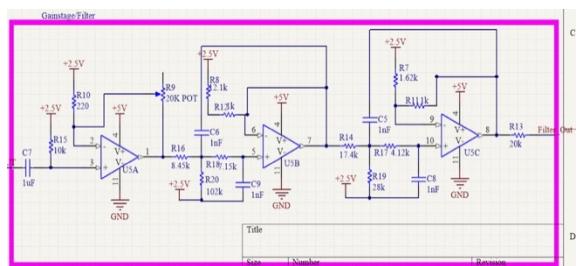
Fig. 9. Signal amplification (Gain stage)

The RF PCB sends out a processed signal (explained below) and receives a new signal after reflecting from the object. The triangle wave from the DAC is sent to the VCO which outputs RF_OUT. The RF_OUT is sent to the attenuator, which outputs the RF_ATTEN signal. The RF_ATTEN signal is sent to the power splitter which contains

RF_LO and the AMP_INPUT. Once the VCO output has been attenuated, the signal is amplified through the flat gain amplifier and transmitted through the transmit antenna. The returned signal is amplified with 4 TAMP-272LN+ LNAs before being sent to the MACA-63H+ mixer. The mixer takes in the amplified signal from the LNAs and the RF_LO signal to send the IF_OUT. IF_OUT is sent back to the baseband PCB for further processing.
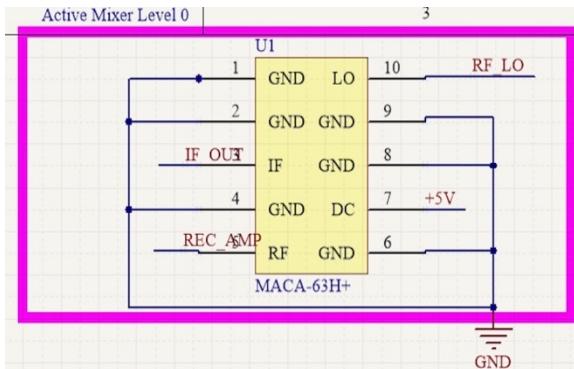
Fig. 10.   Mixer schematic
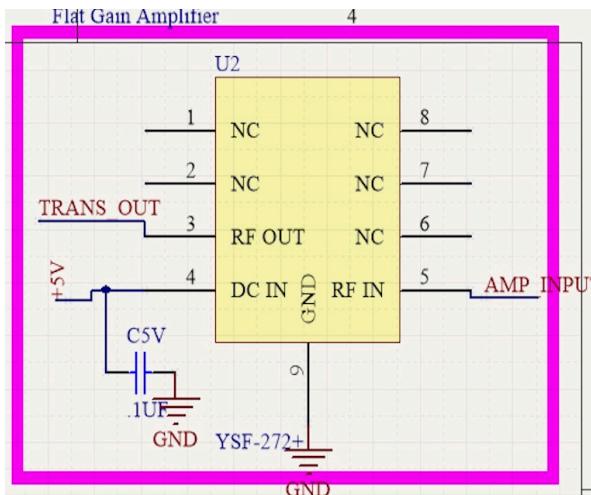
Fig. 11.   Flat gain amplifier schematic
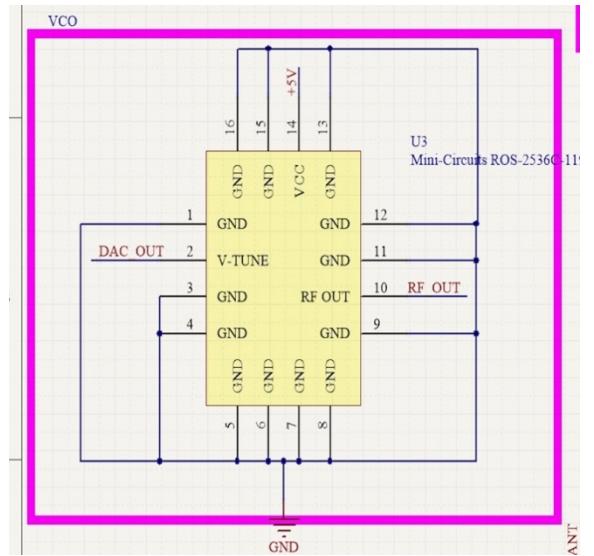
Fig. 12.   Voltage controlled oscillator schematic
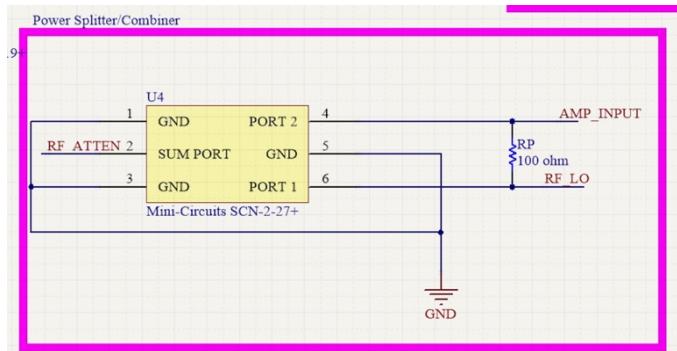
Fig. 13.   Power splitter schematic
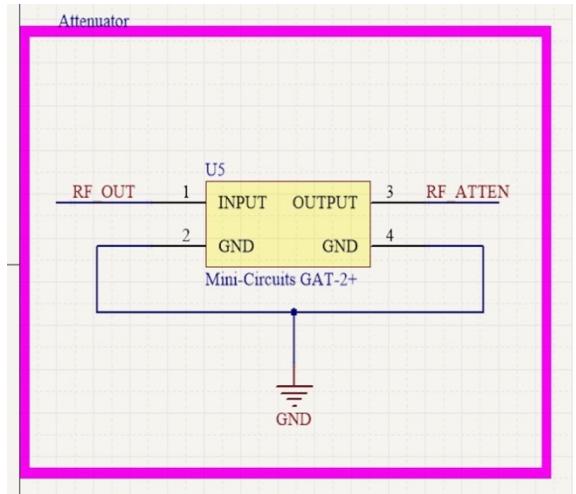
Fig. 14.   Attenuator schematic
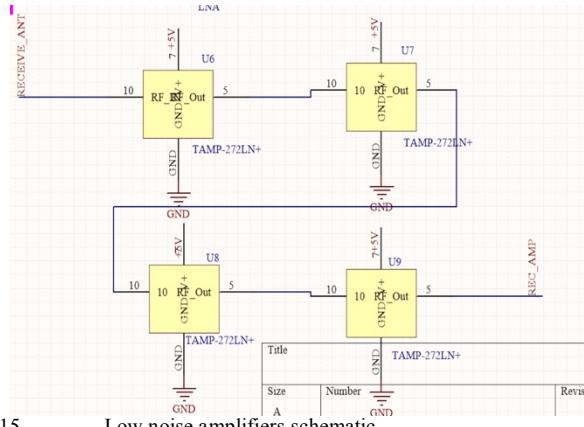
Fig. 15.   Low noise amplifiers schematic

IV. DEBUGGING

We began by soldering on the voltage regulator which included the LM317 and accompanying resistors and capacitors. The voltage regulation section worked by itself but once we included the precision voltage reference section, in addition to the voltage regulator, the voltage input was about 1.3V less than the typical 8V we were expecting to output the necessary 5V and 2.5V. This was due to the distributor who sent us the wrong components that were listed as 220Ω resistors when they were actually some non-essential capacitor values. This issue also plagued our 0Ω resistors, but we could easily detect the culprits after the initial discovery of our 220Ω resistor issue. Once we came to this conclusion, we changed all of the incorrect components for 220Ω and 0 Ohm resistors and both the voltage regulator and precision voltage reference stages worked well in isolation. We made sure to place 0Ω resistors between stages so that we could completely segregate them for testing purposes.

A couple of issues were found with our Baseband PCB while testing. The first error was a misplaced input to the Vref input of our DAC. Instead of inputting the 2.5 V straight into the Vref pin with the capacitors tied from the Vref to ground, we had the 2.5 V in series with the parallel capacitors to the input pin. This error was not found until we tried testing the DAC and discovered that it was not getting the 2.5 V it needed. Instead of filtering out voltage noise as it was designed to do, the capacitors acted as open circuits at DC, thus preventing the 2.5 V from ever powering the DAC. Also, an additional attenuator was added at the output of the DAC by accident which needed to be removed.
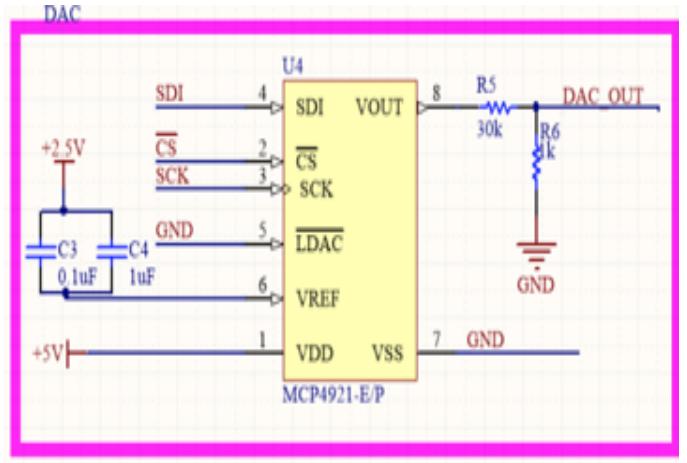

Fig. 16.   Incorrect schematic for DAC input and output
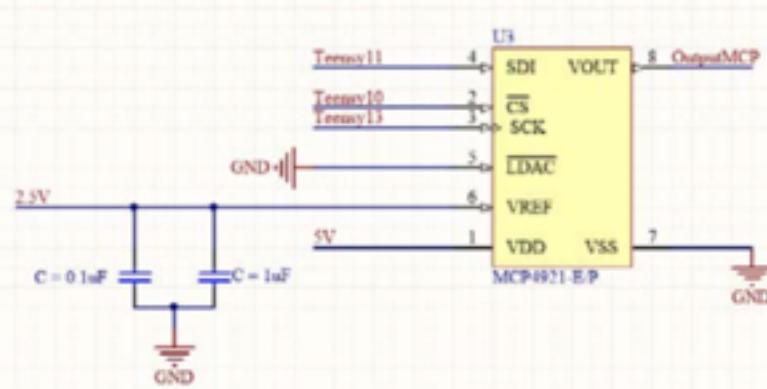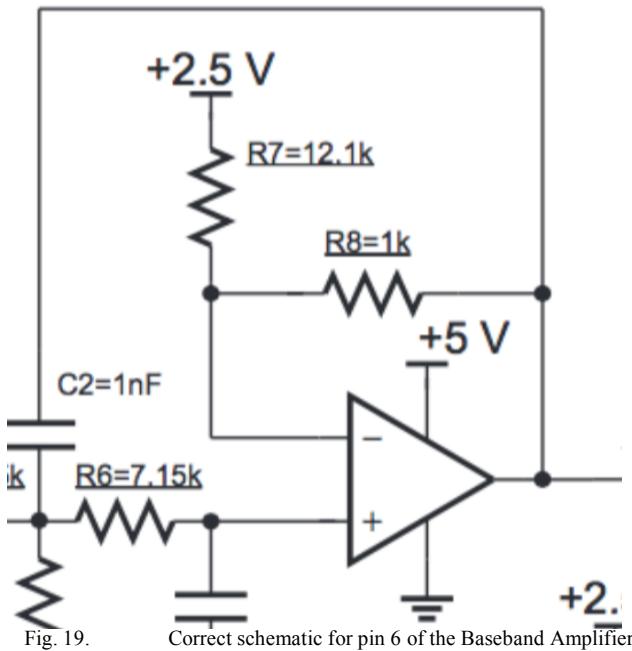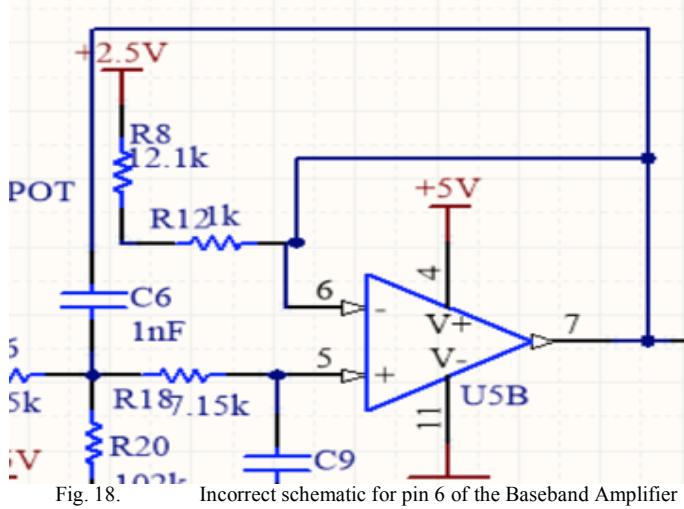
Fig. 17.   Correct schematic for DAC input and output

To fix the misplaced capacitor issue, we decided to use a 0Ω resistor in place of one of the capacitors and leave the other misplaced capacitor open. This would allow the Vref pin of the DAC to get the 2.5 V it needs. Similarly, a 0Ω resistor was used to replace the 30k ohm resistor at the output of the DAC to prevent our DAC output signal from being attenuated.

Before we discovered the issue with the op-amp input and our system was still outputting 2.5V and 5V, we considered using our quarter 1 PCB with a working gain stage. We spent a significant amount of time testing the gain stage with quite a bit of success, but the input to our quarter 1 system was faulty and ultimately failed because it was too small to connect directly to the SMD op-amp.

Another issue we discovered when testing the baseband PCB was a misplaced resistor in the gain stage. This misplaced resistor caused significant power issues that not only affected the gain stage, but every component that needed 2.5V as well. When the gain stage was disconnected from the system, we were able to get the proper 2.5 Volts out of the voltage reference circuit and a proper DAC output. However, once we connected the gain stage, the 2.5 Volts dropped to

around 1.7 Volts which caused our PCB to stop working properly. By isolating the gain stage as the source of the issue we were able to identify the design error causing these power issues. R12 in our gain stage should have been connected from the inverting input of the op amp (pin 6) to the output of the op amp (pin 7) as a feedback resistor instead of connecting the two pins with a short circuit and placing R12 in series with R8. Luckily, pin 6 was not connected at all, so we used a through-hole 1kΩ resistor to connect R8, pin 7, and pin 6 together for negative feedback.

Fig. 18.   Incorrect schematic for pin 6 of the Baseband Amplifier

Fig. 19.   Correct schematic for pin 6 of the Baseband Amplifier

After solving all of the power issues, we began testing voltages and output signals to determine functionality of the overall board. We immediately saw expected results and thought the board was completely working. When we tried to replicate the results of our previous testing after the RF board

was complete, we noticed that we couldn't get a DAC output. We checked the data sheet for the MCP4921 and noticed it has a relatively low maximum input voltage of 6.5V before expiring. Our conclusion was that the voltage regulation was tuned incorrectly, with the potentiometer, to higher than the maximum voltage of the DAC and, therefore, broke the component. This issue stems from the fact that we are using a 5kΩ potentiometer in place of the 2kΩ potentiometer that was supposed to be used for the voltage regulation stage.

After taking out the blown DAC some of the holes on the PCB were damaged so we had to fly wire multiple inputs/outputs from the new DAC to other components on the board. The first fly wire is SDI (pin 4) on the DAC that goes to SDI (pin 11) on the Teensie. The second fly wire is for DAC output (pin 8) and the last fly wire is to the 5V input (pin 1). Once the new DAC was installed, we began by testing the voltages and signal outputs, once again. Changing the DAC fixed the problem and our PCB was working. We began testing the whole system and it was working perfectly.

After some time tuning the system we made the mistake of changing the 5kΩ potentiometer too low again and inputted more than the maximum voltage rating on the DAC, so we had to replace it a second time. This time we added risers so that we could change the DAC on the fly. While taking everything out, more of the PCB was damaged, so we added additional fly wires to make sure all of the connections were complete. This time we had to add both the CS and SCK (pin 2 and pin 3) from the DAC to the Teensie (pin 10 and pin 13) as well as all of the fly wires from the previous fix. At this point, it might have been better off on a breadboard, but it was working decently, albeit fidgety, so we decided to proceed with the current setup.

V. Final Design
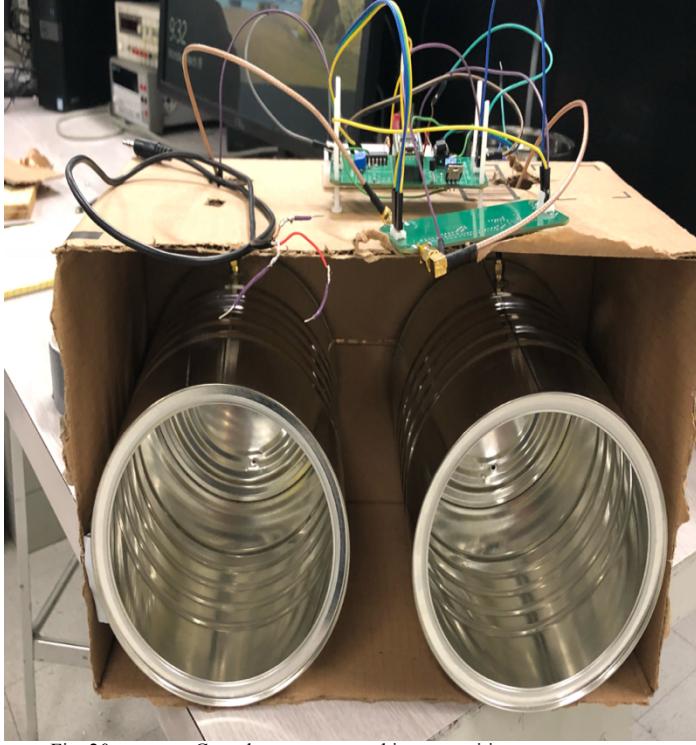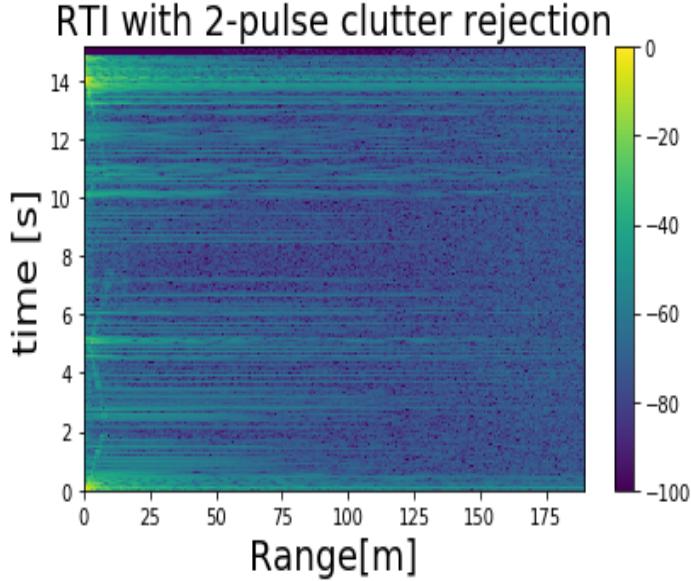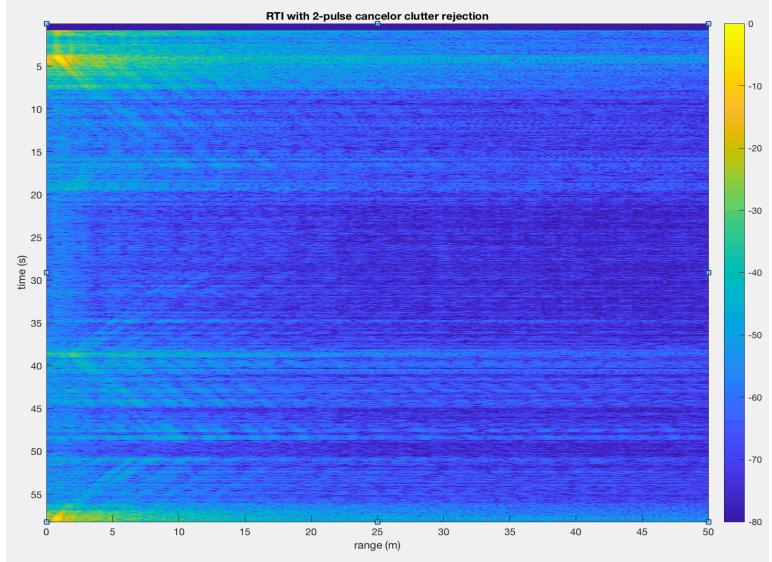
Fig. 20.   Complete system used in competition

VI. Final Results

Results testing in front of Kemper prior to competition day using Python to process .wav file:

Same .wav file processed with Matlab code:

VII. Conclusion

This senior design gave our team great insight into the development of a radar system. Even though low-level design was not covered, the concepts were appropriately covered in lecture. As for practical experience, there was a quite a bit experience gained through designing and debugging boards PCB boards. We had to come up with ideas that could compensate for mistakes that were made on the PCB and for when issues arrived with component selection. Both the baseband and RF PCB had mistakes that needed to be accounted for. Even though these issues were unfortunate, it allowed our team to use techniques that are commonly used to debug PCB's. It also gave the hindsight for future fabrication. Test points and other pins would have been useful when testing the RF board. Issues with component selection allowed us to be able to come up with systems that can compensate for it. For example, the VCO, we created a dc offset system so that it can operate within in the right ranges of frequencies that the original system was designed for. Overall the issues we faced, gave us valuable experience with debugging PCBs.

References

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