EEC 134 Final Report Team TEAM

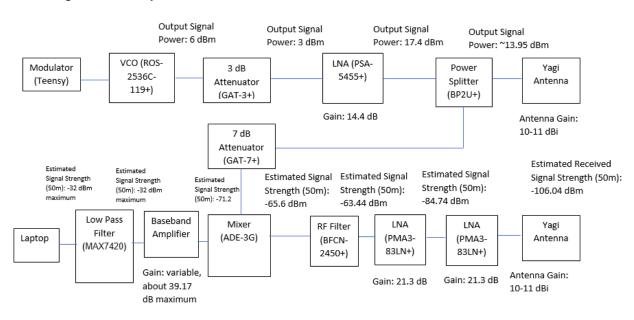
David Fisher Lap Hoang Gabriel Mendez Scott Richards

Abstract

This report details the design, implementation, and testing of a Frequency Modulated Continuous Wave (FMCW) radar system. This sort of radar system transmits a continuous signal and receives a reflection of the original signal which can then be used to determine either the position or speed of an object based on the difference in frequencies of the two signals. After building a radar system whose design was provided to us in the first quarter of the class, our goal was to improve upon this design in the second quarter. This was primarily done by selecting different components that we believed could improve upon the original design.

Design of the System

This system has two primary subsystems: a transmitting system, and a receiving system. The transmitter consists of a modulator, a voltage controlled oscillator (VCO), an attenuator, a low noise amplifier (LNA), a power splitter, and a transmitting antenna while the receiver consists of a receiving antenna, two LNAs, an RF Filter, a mixer, a baseband amplifier, a low-pass filter (LPF), and a computer for processing the final signal. Below is a block diagram of the system:



In regards to selecting the components, we had several desirable qualities we looked for. The first and most obvious is that the components used operated at the frequencies of the signals we would be using, which were 2.4 GHz for the transmitting portion and slightly higher than 2.4 GHz for the receiving portion depending on the position of the object being observed. Next, the supply voltage was a concern. Since we were only allowed to use one power supply, we wanted to have as many components as possible use the same supply voltage. Although we could build circuits that provided other biases other than the primary supply voltage such as a voltage regulator or a voltage reference circuit, we decided against this for providing power to components as it would require more circuitry and thus more things that could go wrong, a potentially harder time troubleshooting any problems, more power consumption, a higher cost, and a heavier system. As such, a supply voltage

of 5 volts was selected for the whole system. Third, the power of the signal at different stages was looked at so that the signal did not clip and could be properly processed in the final stage of the receiving end. Using ADIsimRF to simulate the transmitting and receiving subsystems of the radar system, the components were tested to make sure that they would not distort the signals and that the computer would receive a sufficiently powerful but not to powerful voltage. Additionally, an equation that calculates the received power in a radar system was used along with some rough estimations for non-idealities in free-space to estimate the received signal strength. The ADIsimRF simulation for the transmitting side is below:

ADISimRF -	-	-															-		>
<u>File</u> <u>S</u> tage	Reference	Data Help																	
AHEAD OF WHAT'S P	CES	5	►			۵]												C
+		Stage 1 🔶	S	tage 2		S	tage	3	Þ										
		two t			≻		-	}											
Transm	út	Atten 💌	LNA			Devio	e		•										
Toggle Tx	/Rx	Temp Part 💌	Temp	Part		Temp	Part		•										
Output Freq	(MHz)	2400	2400			2400													
Zin	(Ohms)	50	50			50													
Cout			50			50													
Power Gain	(dB)	-3	14.4			-3.4													
/oltage Gain	(dB)	-3	14.4			-3.4													
DIP3	(dBm)	100	32.2			100													
OP1dB	(dBm)	90	18.5			90													
Pout	(dBm)	3	17.4			14													
out Backoff	(dB)	87	1.1			76													
Peak Backoff	(dB)	87	1.1			76													
Noise Figure	(dB)	0	1			0													
/oltage	(V)	0	0			0													
Current	(mA)	0	0			0													
		Input					Ana	lysis-											
		Number of Sta	iges	3					t Power (rms)		dBm	Noise Figure	1.81	dB		OIP3	28.8	dBm	_
		Input Po		6	dBm				Voltage (rms)		Vms	Output NSD				IIP3	20.8	dBm	
		Analysis Bandy		1	Mhz			Outpu	t Voltage (pp)		Vpp	Output NSD	1.4	nV/rtHz	-	IMD(Po/2 per tone)	-35.6	dB	_
		PEP-to-RMS F		0	dB				OP1dB IP1dB	15.1 8.1	dBm dBm	Output Noise Floor SNR	-104.2 118.2	dBm dB	$\left\{ \right\}$	SFDR ACLR (est.)	88.5 -50	dB dB	-
		P1dB Backoff War Peak Backoff War		1	dB dB				Power Gain	8.1	dB	SNR	110.2	00	' -	Pwr Consumption	-50	W	-
		reak backoff War	ning		ub		1 L		i onel dalli	8	dB					- m consumption	~		

ADISimRF -	134_Receive	r_fixed.sgc																	- 0	×
Eile Stage	Reference	Data Help																		
AHEAD OF WHAT'S P	LOG CES				\$															0
+	•	Stage 1	Stage 2	2	Stage 3	-> St	age 4	•	Stage 5		Stage 6		Stage 7		Stage 8		Stage 9		Stage 1	0
				~	BPF	- (\otimes		Gain	-	- LPF	-			-				-	}
Receiv	e	LNA 💌	LNA	-	BPF	▼ Mixer (F	k)	▼ Gain	Block	▼ LPF		-	Device	▼ D	levice	•	Device	-	Device	•
Toggle Tx	r/Rx	Temp Part 🔹	 Temp Part 	-	Temp Part	▼ Temp F	art	▼ Temp	Part	▼ Terr	ip Part	-	PartNumber	▼ P	artNumber	•	PartNumber	-	PartNumber	•
Input Freq	(MHz)	2400	2400		2400	2400		0		0										
Zin	· · · · · · · · · · · · · · · · · · ·	50	50		50	50		50		50										
Zout		50	50		50	50		50		50										
Power Gain	(dB)		21.3		-2.2	-5.6		39.2		0										
Voltage Gain	(dB)		21.3		-2.2	-5.6		39.2		0										
IIP3	(dBm)	30	30		102.2	105.6		60.8		100										
IP1dB	(dBm)	19.1	69.7		93.2	96.6		51.8		91										
Pin	(-106	-84.7		-63.4	-65.6		-71.2		-32							ļ			
Pin Backoff		125.1	154.4		156.6	162.2		123		123							ļ			
Peak Backoff	(dB)	125.1	154.4		156.6	162.2		123		123							ļ			
Noise Figure	(dB)	0	0		0	0		0		0										
Voltage	(V)	0	0		0	0		0		0										
Current	(mA)	0	0		0	0		0		0										
		Input			Analy															
)utput Power (rm	s) -32	dBm		Noise Figu	re 0	dB			DIP3 82.51	dBm				
		Number of S	-	10		itput Power (m itput Voltage (m		mVms		Output NS		dBm/H	7		IIP3 82.51	dBm				
		Input I Analysis Band		dBm Mhz)utput Voltage (p		mVpp		Output NS	_	uV/rtH				dB	-			
		PEP-to-RMS		dB		OP1		dBm	Outp	ut Noise Flo	or -40	dBm			FDR 81.6	dB				
		P1dB Backoff Wa		dB		IP1	IB 12.8	dBm		SM		dB		ACLR (est.) -8	dB				
		Peak Backoff Wa	-	dB		Power Ga	_	dB	Input	Rx Sensitivi	ity -104	dBm	Pwr C	onsump	otion 0	W				
		Min S/N for D	Demod 10	dB		Voltage Ga	in 74	dB												

Similarly, the simulation for the receiving side is as follows:

The used received power equation for a radar system and the estimations for the received power using estimated non-ideal losses are as follows:

$$P_R = \frac{P_T G_T G_R \lambda^2 \sigma}{(4\pi)^3 R^4}$$

Additionally, the estimated loss from various sources was 21.1 dBm. From this, we made the following estimations for the received power:

Distance (m)	Power Received without Loss (dBm)	Power Received with Loss (dBm)
5	-41.06	-62.16
50	-84.94	-106.04

Moreover, other qualities used to determine the components used were the power consumption of the component, the cost of it, the weight of it, any loss caused by the component, and any noise associated with it. Also, we primarily selected components from

Minicircuits to simplify looking for parts and since we felt that Minicircuits had more detailed or clearer datasheets than some of the other manufactures.

Now, we will look at the transmitting end of the system. For the modulator, we used the Teensy 3.1 chip provided to us in the first quarter. Next, a ROS-2536C-119+ VCO from Minicircuits was chosen for the VCO. We found that the transmitted signal needed to be attenuated slightly to avoid distortion later in the LNA stage, so a GAT-3+ attenuator was used in the transmitting end. An LNA was needed in the transmitting side of the apparatus for which we chose a PSA-5455+ from Minicircuits as it provided what we believed would be adequate signal amplification and a high enough 1dB compression point to avoid distorting the signal. We also chose to use a TCCH-80+ RF Choke from Minicircuits as part of the recommended application circuit for the PSA-5455+ LNA to help filter any undesired signals interfering with the biasing of the LNA. A BP2U+ power splitter was chosen so that the transmitted signal could be used in the mixer in the receiving subsystem. Finally, a Yagi antenna found online was used for the transmitting antenna. We originally planned to fabricate our own antennas for the project; however, we decided that due to time constraints, it would be more effective to purchase a commercial product with desired qualities. For the antennas we selected, they operated at 2.4 GHz and had an antenna gain of 10 to 11 dBi.

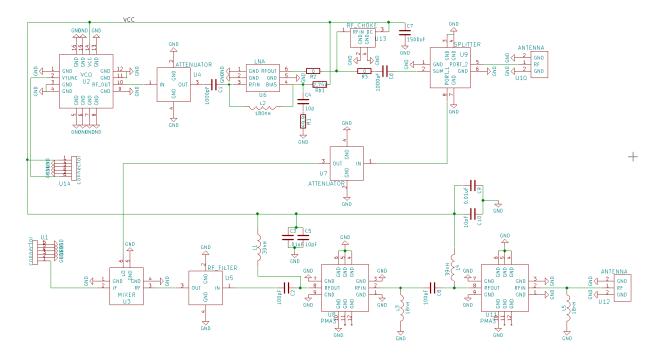
For the receiving end of the system, we chose the following parts. Like the transmitting end, we used a Yagi antenna. Next, we used two PMA3-83LN+ LNAs to provide the gain that we believed would work for the receiver. TCCH-80+ RF Chokes were again used as suggested by the recommended application circuit. An RF filter was then chosen to remove any unwanted received signals. For this, we used a BFCN-2450+ filter. An ADE-3G mixer was used to mix the received and transmitted signals to get a low signal signal with the transmitted signal being the LO signal. Also, a 7 dB attenuator, specifically using a GAT-7+, was needed to match the power of the LO signal to the level of the mixer which was a level 7 mixer. The IF signal from the mixer was then processed by a baseband system modeled on the Quarter 1 baseband system.

The other part of the system was the baseband amplifier. The baseband amplifier contained two parts. The first part was the LDO voltage regulator that maintained a constant voltage of 5V for the system. This LDO was the TPS737 and was used to create a constant voltage and had a voltage divider to create a 2.5V reference for the negative inputs of the amplifier. The Teensy 3.1 was used to produce a square wave of 2 Vp-p that went to the MCP4921 DAC to produce a triangle wave. That triangle wave goes to the V-tune of the VCO to produce the 2.4 GHz signal.

The IF signal of the mixer was amplified by one stage of the the TL974N. This amplified signal was amplified about 40 times and was then filtered by a MAX 7420 low pass filter. This filter is tuned by a clock tunable frequency to match the 15kHz that is expected to be filtered. This was tuned by the 73pF attached to the clock of the filter. This filtered signal was then recorded by Audacity and processed by Matlab.

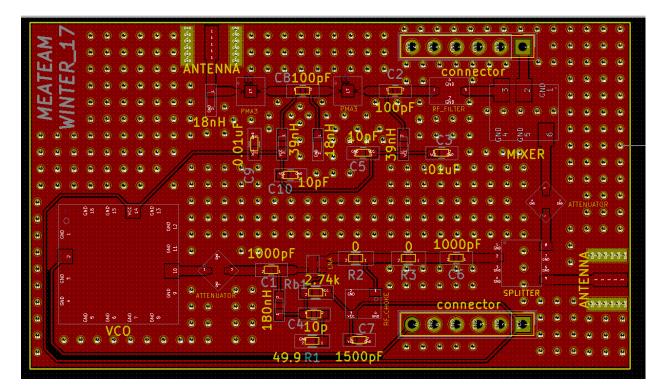
PCB Design

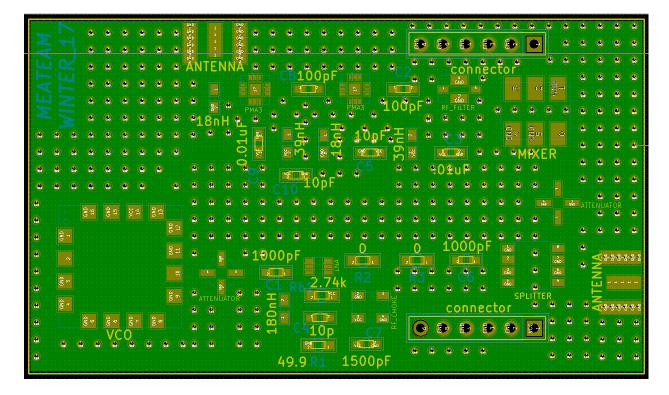
For the PCB design of the radar, we decided to make two separate PCBs, one PCB was for the RF sub-circuit and the other one was for the baseband sub-circuit. We planned to stack two PCBs using two sets of pin headers placed parallel with other to share the common signals such as voltage supply Vs, ground GND, and IF output. Additionally, we used the parallel structure to support the PCBs when we stacked them up, making the system more structurally stable. Separating the whole system into two sub-circuits helped simplify the circuit design since the RF and the baseband sub-circuits had different requirements and parameters that need to be concerned. For example, the RF board needed all the traces on the top layer of the PCB while this limitation was not extended to the baseband board. Also, the RF PCB dealt with transmission lines, so we needed to apply a via fence on the board to prevent any interfering signals from surrounding environment: however, the baseband PCB did not require this kind of work. Separating the circuit was also helpful for the testing purposes. We could put some test points on the baseband board to test the performance and function at critical points on the circuit; however, this was not possible on the RF board. KiCad was the software that we used to design the PCBs, its basic functions were introduced to us in the first guarter of the course and we had the chance to practice on several simple PCBs, giving us enough experience and knowledge to make our own designs.



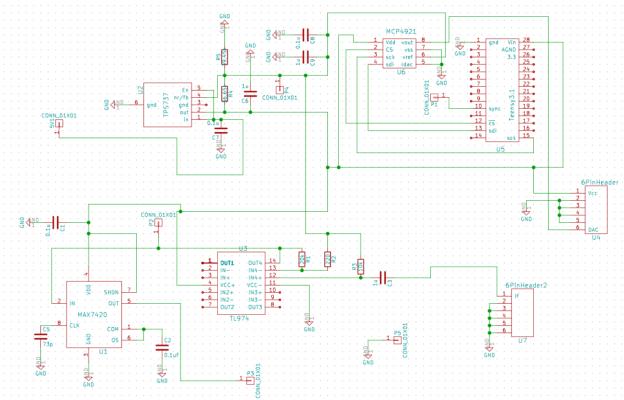
The RF PCB design is presented as follows. First, the schematic of the RF board:

Next, the top layer of the RF board:

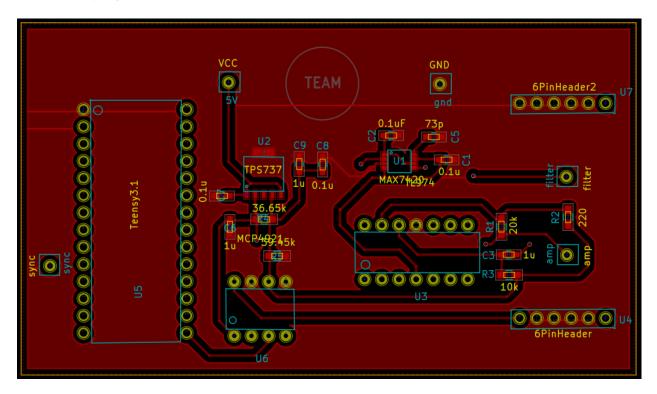




Finally, the bottom layer of the RF board:

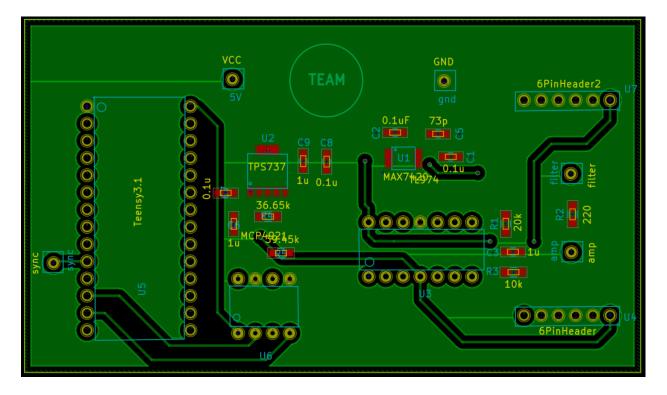


The Baseband Amplifier PCB design is presented as follows. First, the schematic of the RF board:



Next, the top layer of the Baseband board:

Finally, the bottom layer of the Baseband board:



The DFM report of the RF board, as generated by Bay Area Circuits, is presented as follows:

Name		3924k2q	6.zip			ld.			8329	9 - QED W	th Ima	age Data
Report Generated	d on	-	-	2:21:31 AM	1	Customer				antDFM	68 - B	0
Board Id					<u> </u>		с					
Single PCB View	_		_	-		_	_	-		-		_
	To	p View	-		-			Bo	ttom Viev	N	_	
1.500 besh MEATEAN WINTER 17		C2 C5 C5 C5 C5 C5 C5 C5 C5 C5 C5 C5 C5 C5	3 C6				00000		2.7100 Inch			
Summary - Gener	al								11			
PCB Size		2	2.710	0 inch x 1.5	600	inch Copper	Layers					2
PCB Thickness				e	62.00) mil Solder I	Mask					Both
Customer Panel S	Size					Solder	Mask Color					Green
SMD Pads Top						148 Legend						Top Only
SMD Pads Bottor	n					0 Legend	Color					White
SMD Density Top	1			35 SM	∕ID/ir	nch ² Peeloff	Mask					None
SMD Density Bot	tom			0 SM	∕ID/ii	nch ² Carbon	Mask					None
Number of Nets						26 Drill Ho	e Density				1	103 Holes/inch ²
Electrical Test				Sing	le S	ided Holes in	SMD Pads					Yes
Max. Aspect Ratio	o on PTH					6.2 Edge C	onnectors					No
Summary - Coppe	er Layers											
Layer Type	Min. Line V		Mir	n. Ring	Mir	n. Clr. to Copper	Min. Clr. to Pl Hole		Min. Clr.	to NPTH	Min.	Clr. to Outline
	6	mil		mil	9	mil	0	mil		mil	10	mi
Outer	-	9.00		12.00		5.32		18.00				8.95
Inner			_									
Summary - Seque												
Туре	Sequences	Tools		Min. End D	Dia. mil	Max. End Dia. mil	Holes		Ring on uter mil	Min. Ring Inner	, on mil	Min. Clr. Hole to Copper mi
Blind	0						1	-				
Buried	0											
PTH	1		3	10	0.00	39.00	434		12.00			18.00
Plated (Total)	1		3		0.00	39.00	434		12.00	1		18.00
NPTH	0											
Total	1		3	10	0.00	39.00	434	-	12.00	_	_	18.00

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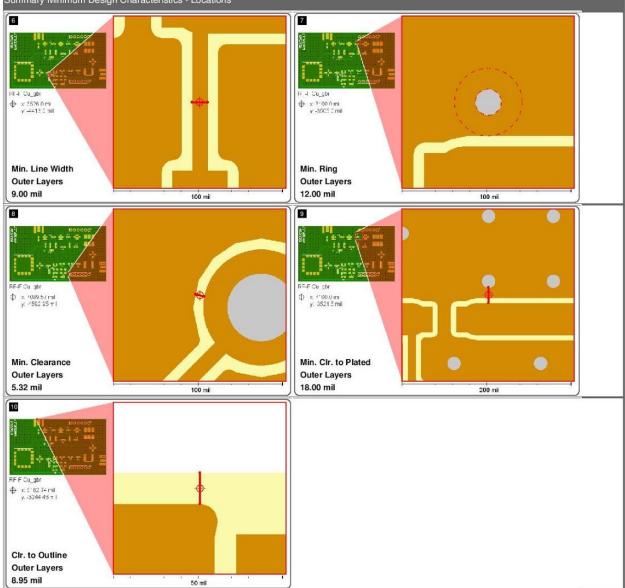
Page1

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QED Report

Integr8tor

Name	3924k2q6.zip	ld.	8329 - QED With Image Data
Report Generated on	Feb 4, 2017 12:21:31 AM	Customer	InstantDFM
Board Id			



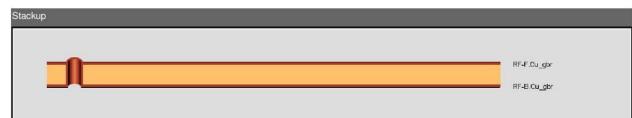
Summary Minimum Design Characteristics - Locations



QED Report

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Name	3924k2q6.zip	ld.	8329 - QED With Image Data
Report Generated on	Feb 4, 2017 12:21:31 AM	Customer	InstantDFM
Board Id			



Copper Layers										
File	Pos.	Min. Line Width	Min. Ring	Min. Clr. to Copper	Min. Same Net spacing	Min. Clr. to Plated Hole	Min. Clr. to NPTH	Min. Clr. to Outline	Copper Are	ea
		mil	mil	mil	mil	mil	mil	mil	inch ²	%
RF-F.Cu_gbr	1	9.00	12.00	5.32	16.06	18.00		8.95	3.9465	93
RF-B.Cu_gbr	2	>16.00	13.55	5.32	>20.00	19.28		8.95	4.1462	98

Drill Tools														
File	Tool Nr.	Span	Туре	Method	FilledVia	Countered	End Dia.	Holes (in PCB)	Moves (in PCB)	Double Hits (in File)		Min. Ring on Outer	Min. Ring on Inner	Min. Pad Size
							mil					mil	mil	mil
RF_drl	1	1-2	PTH	unknown	unknown	unknown	10.00	24	0	0	0	16.05		42.10
RF_drl	2	1-2	PTH	unknown	unknown	unknown	15.00	398	0	22	0	12.00		39.00
RF_drl	3	1-2	PTH	unknown	unknown	unknown	39.00	12	0	0	0	13.96		66.92

Sequenc	ces											
Span	Туре	Tools	Min. End Dia.	Max. End Dia.	Holes	Min. Ring on Outer	Min. Ring on Inner	Min. Ring on Outer NPTH	Min. Ring on Inner NPTH	Min. Clr. Hole to Copper	Min. Clr. Hole to Outline	Min. Clr. Track to Outline
			mil	mil		mil	mil	mil	mil	mil	mil	mi
1-2	PTH	3	10.00	39.00	434	12.00				18.00	22.50	disabled
All	Plated	3	10.00	39.00	434	12.00				18.00	22.50	disabled
All	All	3	10.00	39.00	434	12.00				18.00	22.50	disabled

Rout Tools						x=
File	Tool Nr.	Туре	Tool Dia.	End Dia.	Draw Length	Nibble Count
			mil	mil	mil	

Routed Holes						
File	Hole Nr.	Instances	X Size	Y Size	Draw Length	Nibble Count
			mil	mil	mil	



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OED Report

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Name	3924k2q6.zip	ld.	8329 - QED With Image Data
Report Generated on	Feb 4, 2017 12:21:31 AM	Customer	InstantDFM
Board Id			

Solder Mask							
Side	Min. Ring on Cu Defined Pads	Min. Ring on SM Defined Pads	Min. Clr. Mask to Mask	Min. Web	Min. Clr. Mask to Copper	Fully Covered Via Holes	Partly Covered Via Holes
	mil	mil	mil	mil	mil		
Тор	7.87		3.25	1.75	6.63	Yes	No
Bottom	7.87		>10.00	>10.00	>10.00	Yes	No

Initial	Renamed	Format	Function	Position	Color
RF-F.SilkS.gbr	RF-F.SilkS_gbr	ger274x	silk	top	white
RF-F.Mask.gbr	RF-F.Mask_gbr	ger274x	mask	top	green
RF-F.Cu.gbr	RF-F.Cu_gbr	ger274x	outer	1	
RF-B.Cu.gbr	RF-B.Cu_gbr	ger274x	outer	2	
RF-B.Mask.gbr	RF-B.Mask_gbr	ger274x	mask	bottom	green
RF.drl	RF_drl	excellon2	plated	1-2	
RF-B.SilkS.gbr	RF-B.SilkS_gbr	ger274x	empty	none	
RF-Edge.Cuts.gbr	RF-Edge.Cuts_gbr	ger274x	cad_outline	none	
report.txt		text	document		

Comments



The DFM report of the Baseband board, as generated by Bay Area Circuits, is presented as follows:

QED I											8tor
Name		dkgm9ft5.zi	P	Id.				9132	- QED Wi	th Ima	ige Data
Report Generated	on	Mar 5, 2017 1	2:19:33 PM	Custo	mer			Insta	ntDFM		
Board Id											
Single PCB View	_	_	_		_				-		_
0	То	p View	_		_		B	ottom Viev	N	_	_
2010 MA			- IO	2 0460 inch				• • • • •	:	[]	0
Summary - Genera	al							_			
PCB Size		3.577	0 inch x 2.0490		per Layers						
PCB Thickness			62.0		ler Mask						Bo
Customer Panel S	ize				ler Mask Color	r					Blu
SMD Pads Top				39 Leg							Top Or
SMD Pads Bottom	1				end Color						Whi
SMD Density Top			5 SMD/		loff Mask						Nor
SMD Density Bott	om		0 SMD/	inch ² Car						Nor	
Number of Nets					Hole Density						10 Holes/inc
Electrical Test			Single 8	Sided Hol	es in SMD Pad	s					1
Max. Aspect Ratio	on PTH			3.9 Edg	e Connectors						1
Summary - Coppe	r Layers										
Layer Type	Min. Line W	/idth Mir	n. Ring M	in. Clr. to Cop	per Min. Clr.	to Pl ole	ated	Min. Clr.	to NPTH	Min.	CIr. to Outlin
	-	mil	mil		mil		mil		mil		n
Outer	5	15.00	3.81		.00					8	32.9
Inner											
Summary - Sequer	nces										
Туре	Sequences	Tools	Min. End Dia.	Max. End D	a. Holes			Ring on uter	Min. Ring Inner	on	Min. Clr. Ho to Copper
			mi	1	nil			mil		mil	1
Blind	0										
Buried	0										
PTH	1	4	16.00			73		3.81			unknov
Plated (Total)	1	4	16.00	40	00	73		3.81			unkno
NPTH	0										
Total	1	4	16.00	40	00	73		3.81			unknov

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QED Report

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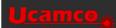
Name	dkgm9ft5.zip	ld.	9132 - QED With Image Data
Report Generated on	Mar 5, 2017 12:19:33 PM	Customer	InstantDFM
Board Id			

Summary Minimum Design Characteristics - Locations 5 6 Min. Ring Min. Line Width Outer Layers Outer Layers 15.00 mil 3.81 mil 100 mil 50 mil 7 8 Min. Clearance Cir. to Outline Outer Layers Outer Layers 6.00 mil 32.95 mil 100 mil 100 mil

Stackup baseband_amp-F.Cu_gbr baseband_amp-B.Cu_gbr

Copper Layers

File	Pos.	Min. Line Width	Min. Ring	Min. Clr. to Copper	Min. Same Net spacing	Min. Clr. to Plated Hole	Min. Clr. to NPTH	Min. Clr. to Outline	Copper Are	ea	
		mil	mil	mil	mil	mil	mil	mil	inch ²	%	
baseband_amp-F.Cu_gbr	1	15.00	3.81	6.00	>20.00	>32.00		32.95	5.6133	77	
baseband_amp-B.Cu_gbr	2	15.00	3.81	29.18	>20.00	>32.00		32.95	5.9064	81	



QED Report

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Name			dk	gm9ft5.zip		I.	ld.				9132 - QE	D With I	mage Dat	а
Report Generated	d on		Ма	ır 5, 2017 12	:19:33 PM	C	Customer			nstant DF	M			
Board Id														
Drill Tools														
File	Tool Nr.	Span	Туре	Method	FilledVia	Countered	d End Dia.	Holes (in PCB)	Moves (in PCB)	Double Hits (in File)	Predrill Hits (in File)	Min. Ring on Outer	Min. Ring on Inner	Min. Pad Size
							mil					mil	mil	m
baseband_amp_ drl	1	1-2	PTH	unknown	unknown	unknown	16.00	6	0	0	0	3.81		23.62
baseband_amp_ drl	2	1-2	РТН	unknown	unknown	unknown	22.00	8	0	0	0	19.00		60.00
baseband_amp_ drl	3	1-2	РТН	unknown	unknown	unknown	30.00	19	0	0	0	15.00		60.00
baseband_amp_ drl	4	1-2	PTH	unknown	unknown	unknown	40.00	40	0	0	0	10.00		60.00

Span	Туре	Tools	Min. End Dia.	Max. End Dia.	Holes	Min. Ring on Outer	Min. Ring on Inner	Min. Ring on Outer NPTH	Min. Ring on Inner NPTH	Min. Clr. Hole to Copper	Min. Clr. Hole to Outline	Min. Clr. Track to Outline
			mil	mil		mil	mil	mil	mil	mil	mil	mil
1-2	PTH	4	16.00	40.00	73	3.81				>32.00	153.00	disabled
All	Plated	4	16.00	40.00	73	3.81				>32.00	153.00	disabled
All	All	4	16.00	40.00	73	3.81				>32.00	153.00	disabled

Rout Tools						
File	Tool Nr.	Туре	Tool Dia.	End Dia.	Draw Length	Nibble Count
			mil	mil	mil	

Bouted Holes

, iour							
	File	Hole Nr.	Instances	X Size	Y Size	Draw Length	Nibble Count
				mil	mil	mil	

Solder Mask							
Side	Min. Ring on Cu Defined Pads	Min. Ring on SM Defined Pads	Min. Clr. Mask to Mask	Min. Web	Min. Clr. Mask to Copper	Fully Covered Via Holes	Partly Covered Via Holes
	mil	mil	mil	mil	mil		
Тор	7.87		>10.00	>10.00	>10.00	Yes	No
Bottom	7.87		>10.00	>10.00	>10.00	Yes	No

Files					
Initial	Renamed	Format	Function	Position	Color
baseband_amp-F.SilkS.gbr	baseband_amp-F.SilkS_gbr	ger274x	silk	top	white
baseband_amp-F.Mask.gbr	baseband_amp-F.Mask_gbr	ger274x	mask	top	blue
baseband_amp-F.Cu.gbr	baseband_amp-F.Cu_gbr	ger274x	outer	1	
baseband_amp-B.Cu.gbr	baseband_amp-B.Cu_gbr	ger274x	outer	2	
baseband_amp-B.Mask.gbr	baseband_amp-B.Mask_gbr	ger274x	mask	bottom	blue
baseband_amp.drl	baseband_amp_drl	excellon2	plated	1-2	
baseband_amp-B.SilkS.gbr	baseband_amp-B.SilkS_gbr	ger274x	empty	none	
baseband_amp-Edge.Cuts.gbr	baseband_amp-Edge.Cuts_gbr	ger274x	cad_outline	none	

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System Testing

Quarter 2 System Failure

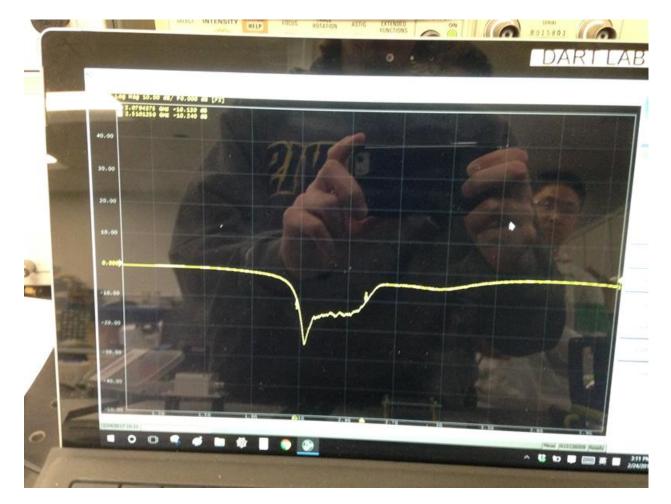
Unfortunately, the system that was designed for the second quarter did not properly operate. We believe that there may have been an error somewhere in the RF PCB, specifically the receiver. For some unknown reason, the two LNAs on the receiving side of the system failed to work and instead attenuated the signal. We thought the failure happened due to the soldering job. The amplifiers ICs were small and had pins at the bottom, so even with the optical equipment provided, it was really difficult for us to verify if we soldered the chips properly or not. Another problem we met is that the inputs of the amplifiers were connected to inductors which were grounded. Thus, we could not confirm whether or not these pins were shorted with the grounded pins nearby. Although the receiver did not work properly, we managed to get the transmitter work fairly well. The transmitting signal which was about 3 dB lower than the expected value, but we could pump that signal up a little higher by taking out the attenuator or adding a gain block. However, due to lack of time and difficulty in pinpointing the problem, we were unable to submit a revised RF PCB in time for the second PCB run.

The baseband PCB also suffered issues. In the first design, there were some issues with some of the connections being wrong as well as some component values that were possibly incorrect. It appeared that pins 5-7 were all grounded and only 5 and 7 should be grounded but pin 6 should receive 2.5V from the voltage divider. The other issue that we saw was that the floor for the amplifier was elevated to 5V so that it appeared to be all DC and no room for amplification of the IF signal. Although we were able to fix the perceived errors in a revised PCB, we did not have time to solder components onto the new PCB as by this point in the quarter, we had moved to focusing solely on rebuilding and improving where we could on the quarter one system.

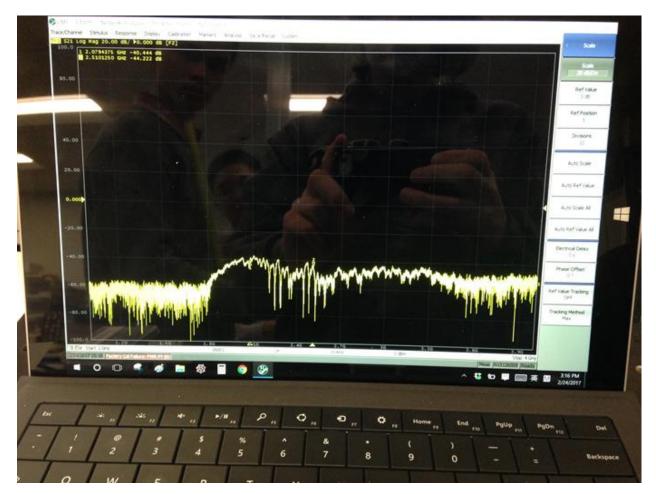
However, we did get proper results for the Yagi antennas we purchased. First, we tested the S11 scattering parameter of each antenna and got an antenna gain of roughly 10 to 11 dBi over the band of frequencies that we were working with. The results are below for the first antenna:

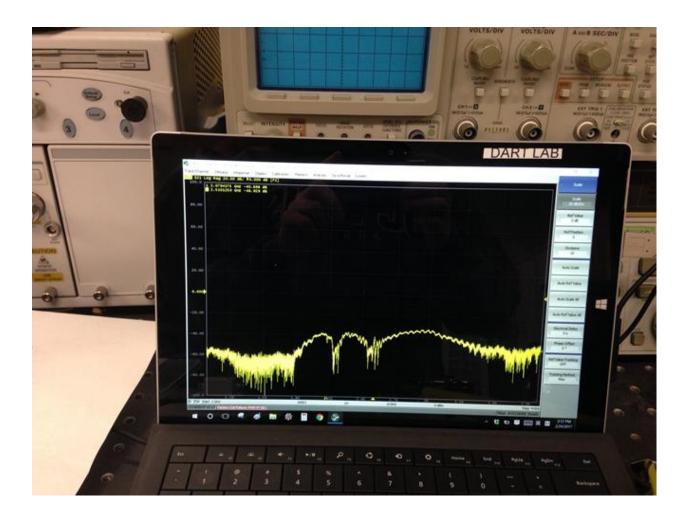


And, for the second antenna:

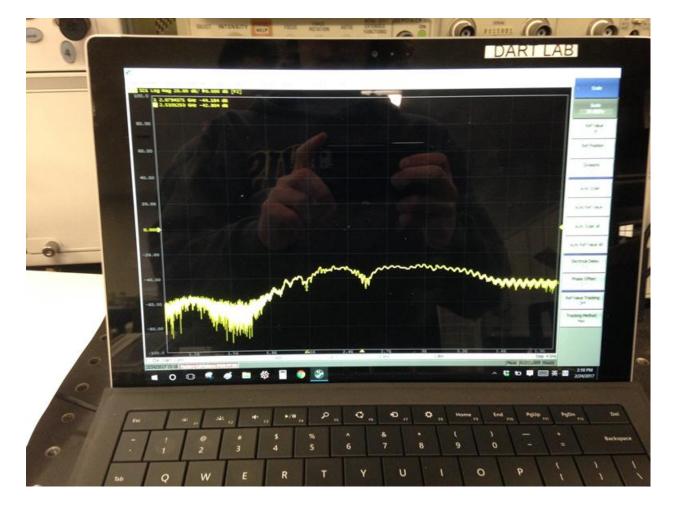


Additionally, we tested the crosstalk of the two antennas to find a good distance to separate them by. We found that having them greater than or equal to a foot apart had crosstalk at a minimum. However, this measurement was not in an anechoic chamber and may not be entirely accurate. First, the antenna S21 with the antennas separated at 12 inches with the two antennas on the same plane:

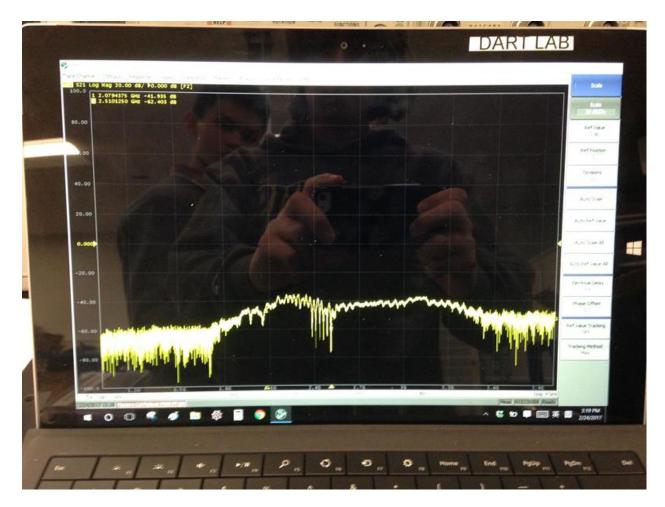




Next, the antennas 12 inches apart with them on parallel planes:



Now, the antennas on parallel planes with them separated by 10 inches:

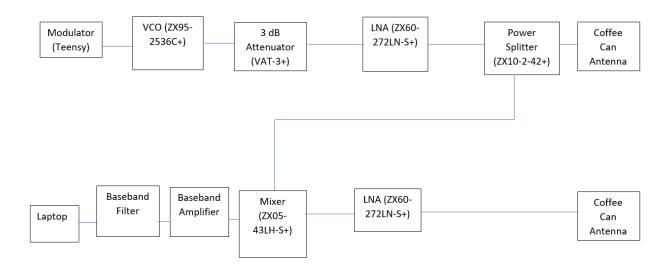


Finally, the antennas separated by 14 inches with them on parallel planes:

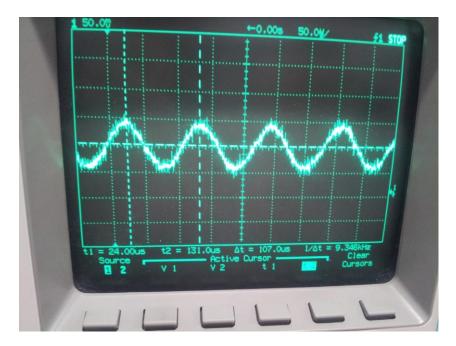
From these measurements, it becomes apparent that the antennas' crosstalk is approximately at a minimum when the two antennas are at least 12 inches apart. As such, we chose to have the antennas separated by at least this distance when assembling the final system.

Quarter 1 System Rebuilding, Modifying, and Testing

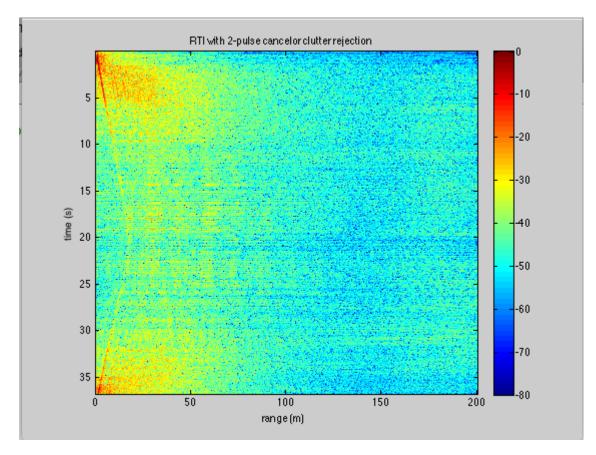
After the failure of our quarter two design, we went with our backup: rebuilding and modifying our system from quarter one. The block diagram of the original quarter one design is as follows:

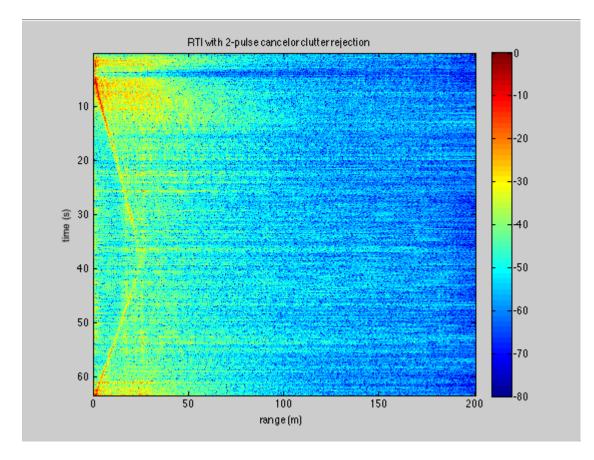


After reconstructing the original design, we tested it by using two TPI synthesizers with one in place of the VCO and the other sending a signal to the receiving end of the system. The first synthesizer was set at 2.4 GHz and the other was set at 2.40001 GHz. This test was done to ensure that we were getting the correct frequency out of the system, and to find the best possible mixer for our system. We obtained a signal with the proper frequency after the mixer as seen below:



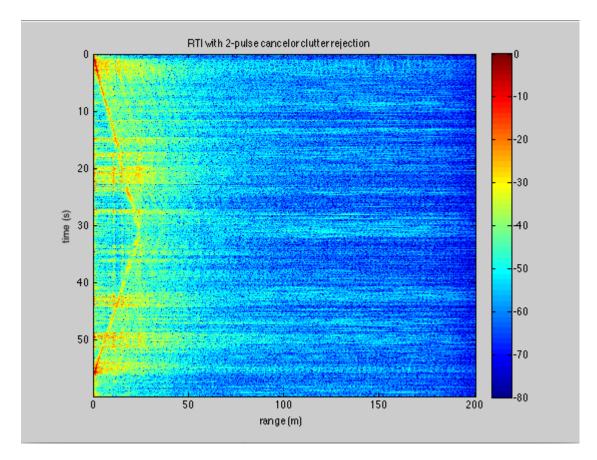
Next, we began making any modifications to improve the system. First, we tested several mixers to replace our original mixer as our original one had an output power that was smaller than anticipated possibly due to some internal problem with it. Next, we added one more LNA. The additional LNA was placed in cascade with the existing LNA of the receiving end right before the mixer to boost the gain of the received signal. Adding the LNA increases the amplitude of the receiving signal, so it is easier to discern the signal with background noise and collect the data needed for processing. Additionally, we removed the 3-dB attenuator in order to maximize the gain in the transmitting side of the system despite the risk of the signal becoming distorted. Also, we compared using the coffee can antennas used in quarter one and the Yagi antennas we purchased in quarter two. We found that using two coffee cans seemed to yield the best results as the Yagi antennas seemed to require being very precisely aimed at the target object. We tested the system indoors in a corridor that was slightly less than 30 meters long. We obtained the following two sets of data with coffee can antennas:





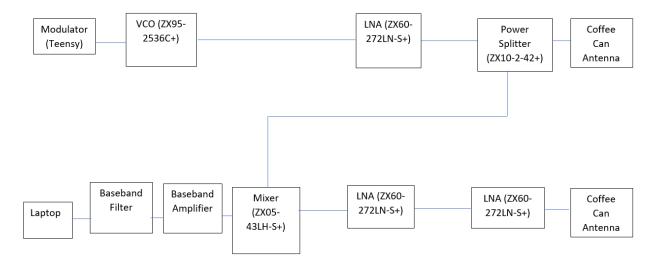
From this data, it is evident that we were able to obtain a signal from approximately 30 meters away.

We also tested the system using a Yagi antenna as a transmitting antenna and a coffee can antenna as a receiving antenna. However, we felt that this run produced inferior results compared to the previous run. The result from this trial is below:



While this test produced similar results, we saw some distortion in the signal. As such, we elected to use coffee can antennas for both antennas.

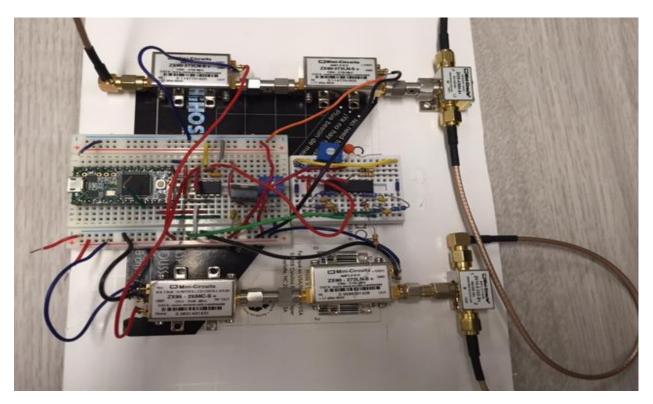
Unfortunately, we were unable to perform a proper outside test with the system because of difficulty obtaining a computer to run the tests on and rain.



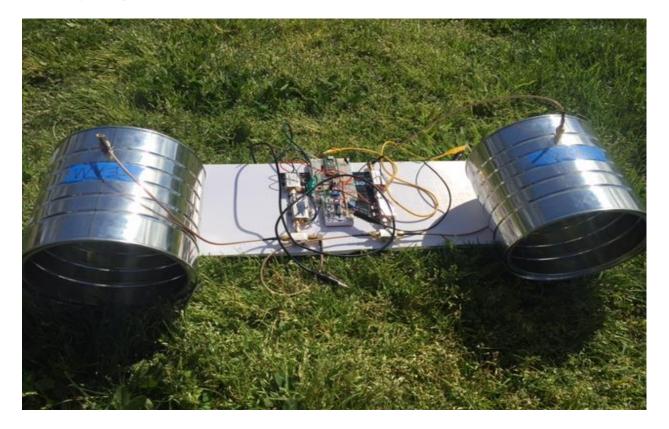
The final block diagram of our system is below:

Pictures of our system are presented below:

Close-view of the final system:



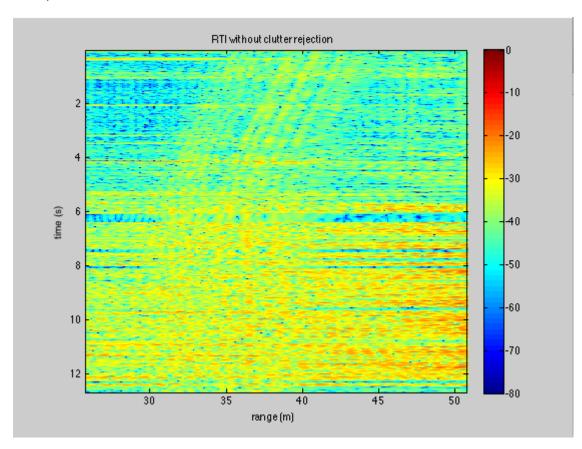
The complete system:



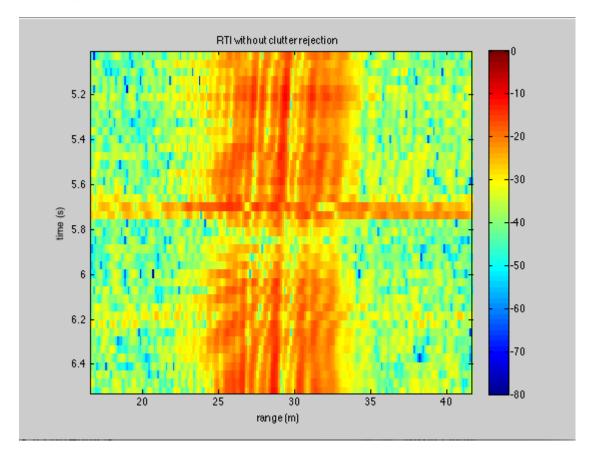
Competition Results

Using our rebuilt and modified Quarter 1 system, we obtained the following results in the radar competition: 36m, 29m, 24m, 19m, and 11m, respectively. The graphs were zoomed in to get the most precise value and are presented as follows:

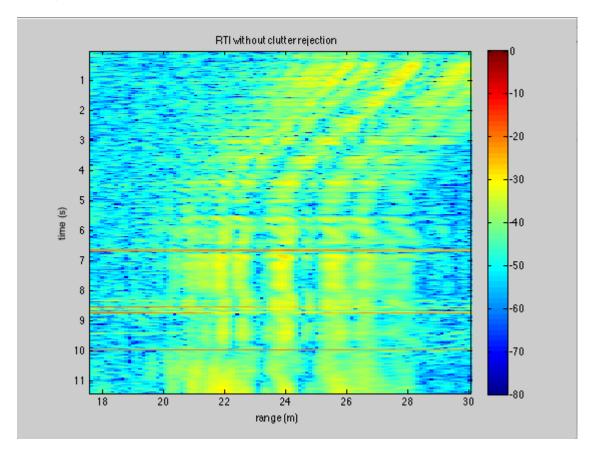
First position:



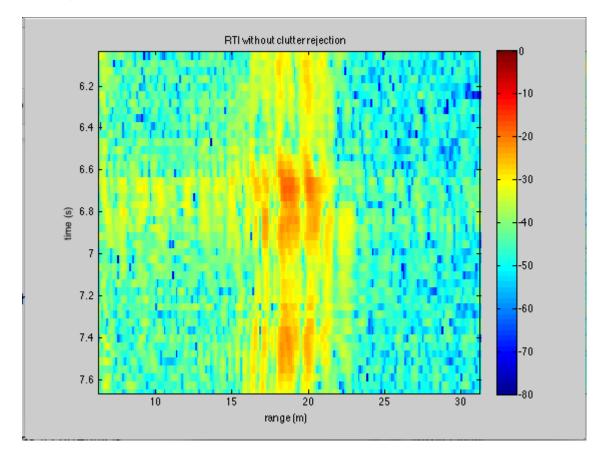
Second position:



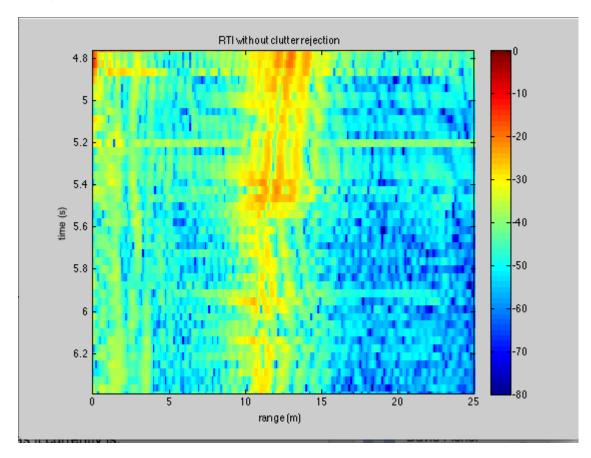
Third position:



Fourth position:



Fifth position:



Although we were able to identify a signal in the received data, the data had much more noise than previously. It's possibly that some part of the circuitry such as the potentiometer in the baseband system was altered when the system was transported to the field where the system was tested, leading to the system not being properly calibrated. Additionally, there may have been noise introduced by the different surroundings. For example, when testing indoors, the system was placed in front of a wall. This placement may have provided less variable interference from objects behind the system, resulting in a more readable result than what was obtained in the final competition.

Discussion

Unfortunately, we were unable to get our second design working. This was most likely due to some error with the PCB design. However, we were able to reconstruct our Quarter 1 system and have it function.

By reusing and modifying the system from the first quarter, we were able to build a working system. We were able to build a system that could detect objects approximately 50 meters away and roughly discern their location.

However, we did experience a large amount of noise in our radar competition results for an unknown reason. Despite this, we were still able to obtain understandable data for the test. Because of these shortcomings, there are certainly ways that we could improve upon the system and the results that we were able to obtain.

Possible Improvements For the System

Although we were able to yield proper data with our system, there is always room for improving it. Several ways in which we could improve the system are discussed as follows.

The first way is to move both the baseband and RF systems to PCBs. Although this was attempted, there were issues with the assembly and testing of the PCBs. Having individual modules for each stage would be helpful in the debugging process since it is unclear which stage is having the issue. This problem could be overcome by having additional time as well as having more PCB prototypes.

Next, better antennas could be used for the system. The coffee can antennas were able to get results; however, the antennas themselves are crude. Using a better commercial antenna set could improve results.

Third, we could have used better components than what our final design used. Since we resorted to resurrecting our Quarter 1 system, the components used were not what we ideally wanted to use. As such, results could improve if we were not limited to these reused components. Additionally, some of the components that we had did not necessarily function as ideally as indicated on their respective datasheet. For instance, we used several mixers before we were able to find one that gave us usable results as the other ones we tested had a much larger loss than what was indicated on the datasheet for the part.

Suggestions For Improving the Class

One suggestion that we have for the class is to possibly merge a couple of the labs in the first quarter. Specifically, we felt that Lab 3 and Lab 4 were very quick and simple labs and could easily be lumped into one lab. We feel that this could benefit future students as it would allow for an extra week in the quarter that could be used to work on Lab 6 as that lab seemed like it was crammed into the end of the quarter.

Additionally, for the second quarter, there could be a better system for getting access to the Fujitsu laptop for testing purposes. For instance, there could be a form for reserving the computer at a certain time for testing or a checkout sheet.

Another suggestion could be having PCB 1 due right from the start of the second quarter since there was a lot of wait time when ordering the PCB. Since the PCB 1 return and PCB 2 design submission were fairly close in timeline, this didn't allow enough time for testing between PCBs.

Conclusion

In conclusion, we were able to build a working FMCW radar system that could detect objects approximately 50 meters away. Although we needed to scrap any design plans

that we had made during the second quarter due to problems with assembling the new system, we still managed to built something that provided results. Moreover, this project has given each of us insight into the operation of a radar system and the general design process for designing a system in Electrical Engineering. Some general notions of system design that this project exposed us to were selecting components to meet specifications, budgeting a system, designing PCBs, and prototyping and debugging a system.

Bill of Materials

Part	Value	Quantity	Description	Price
C_0603_HandSoldering	0.1 u	4	C1, C2, C7, C8	Acquired
C_0603_HandSoldering	1 u	3	C3, C6, C9	Acquired
C_0603_HandSoldering	73 p	1	C5	\$0.10
R_0603_HandSoldering	20 k	1	R1	Acquired
R_0603_HandSoldering	220	1	R2	Acquired
R_0603_HandSoldering	10 k	1	R3	Acquired
R_0603_HandSoldering	36.65 k	1	R4	\$0.10
R_0603_HandSoldering	39.45 k	1	R5	\$0.10
MAX7420	MAX7420	1	U1	\$4.54
TPS737	TPS737	1	U2	\$1.59
1x6 Pin Header	N/A	2	U4, U7	Acquired
pin	pin	5	VCC, sync, amp, filter, GND	Acquired
Teensy	Teensy 3.1	1	U5	Acquired
TL974	TL974	1	U3	Acquired
MCP4921	MCP4921	1	U6	Acquired
Total				\$6.43

The Bill of Materials for the Baseband Amplifier:

The Bill of Materials for RF board:

Part	Value	Quantity	Description	Price
C_SMD_HandSoldering	1000pF	2	C1, C6	Acquired
C_SMD_HandSoldering	100pF	2	C2, C8	Acquired
C_SMD_HandSoldering	0.01uF	1	C3, C9	Acquired
C_SMD_HandSoldering	10pF	3	C4, C5, C10	\$0.29 (each)
C_SMD_HandSoldering	1500pF	1	C7	\$1.50
R_SMD_HandSoldering	49.9	1	R1`	Acquired
R_SMD_HandSoldering	0	2	R2, R3	Acquired
R_SMD_HandSoldering	2.74K	1	Rb1	\$0.10
L_SMD_HandSoldering	180nH	1	L2	\$0.11
L_SMD_HandSoldering	18nH	2	L3, L5	\$0.44 (each)
L_SMD_HandSoldering	39nH	2	L1, L4	\$0.10 (each)
MIXER	ADE-3G	1	U3	Sampled
SPLITTER	BP2U+	1	U9	Sampled
VCO	ROS-2536C-119+	1	U2	Sampled
3dB_ATTENUATOR	GAT-3+	1	U4	Sampled
7dB_ATTENUATOR	GAT-7+	1	U7	Sampled
LNA	PSA-5455+	1	U6	Sampled
POWER AMP	PMA3-83LN+	2	U8, U11	Sampled
SMA CONNECTOR	N/A	2	U10, U12	Acquired
1x6 Pin Header	N/A	2	U1, U14	Acquired
RF_CHOKE	TCCH-80+	1	U13	Sampled
RF_BPF	BFCN-2450+	1	U5	Sampled

Total				\$3.66
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Other parts:

Part	Quantity	Price	
Yagi Antenna	2	\$9.99	
Total		\$19.98	

Acknowledgements

We would like to acknowledge Minicircuits for providing parts for our project through both sampling components through their website and through contacts at the company. Specifically, we would like to mention the representative that came to one of the Friday meetings and Janet Hunn.

Additionally, we would like to acknowledge both Professor Leo and the three teaching assistants for the course, Songjie Bi, Daniel Kuzmenko, and Hao Wang, for providing us with an opportunity to work with and understand the development of this sort of system.