Tutorial: Setting up ADF4158 PLL

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This tutorial is about how to set up the ADF4158 Direct Modulation/Waveform Generating, 6.1 GHz Fractional-N Frequency Synthesizer to output a continuous triangular waveform centered at 4 GHz with a bandwidth of 160 MHz as shown in Figure 1.

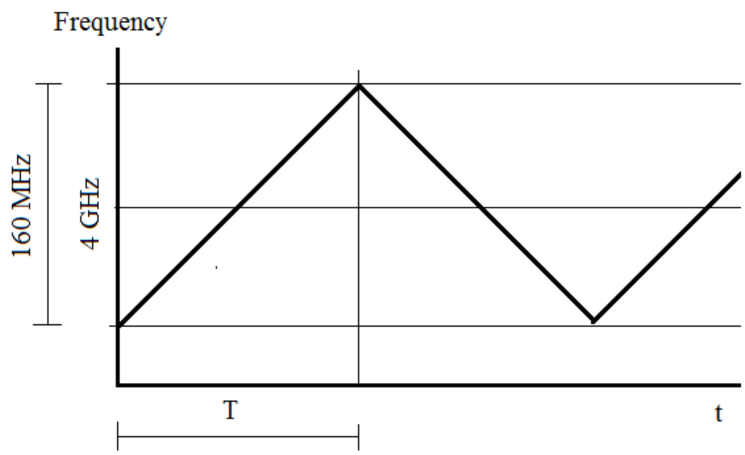

Figure 1: the above figure shows the desired output of the VCO after setting up the PLL.

The following are the values needed to be calculated:

- R
- T
- D
- INT
- FRAC
- f_{DEV}
- DEV
- DEV_OFFSET
- CLK1
- CLK2
- Number of steps

In order to find R, T, D, INT, and FRAC, the following two equations are needed.

$$RF_{out} = f_{PFD} * INT + f_{PFD} * \frac{FRAC}{2^{25}} \quad (1)$$

$$f_{PFD} = REF_{in} * \left(\frac{1+D}{R*(1+T)}\right) \quad (2)$$

First of all, you will need to know the value of your REF_{in}, which is the frequency of the oscillator reference. The PLL can take in REF_{in} range from 10 MHz to 260 MHz, but f_{PFD} has a maximum of 32 MHz. The purpose of D, R, and T is to adjust the oscillator reference to a phase detector frequency less than 32 kHz. D doubles the oscillator reference frequency, T divides the oscillator reference frequency by two, and R divides the oscillator reference frequency by a value between 1 and 32. In our radar design, 40 Mhz of REF_{in} was used, so R = 1, T = 1, and D = 0, which results in f_{PFD} = 20 MHz from equation 2.

Then you will need to set the RF_{out} to the lowest frequency of the triangular wave, which is 3.96 GHz. In order to set RF_{out}, find the value of INT such that $f_{PFD} * INT$ is closest but lower than or equal to your desired RF_{out}. Then use equation 1 to calculate the FRAC value. In our case, 3.96 GHz is divisible by 20 MHz (f_{PFD}), which leads to INT = 192 and FRAC = 0;

The following shows how to calculate for CLK1, CLK2, number of steps, and f_{DEV}.

$$f_{RES} = \frac{f_{PFD}}{2^{25}} \quad (3)$$

$$t_{step_{min}} = \frac{1}{f_{RES}} \quad (4)$$

$$t_{step} = CLK1 * CLK2 * t_{step_{min}} \quad (5)$$

$$number\ of\ steps = \frac{T}{t_{step}} \quad (6)$$

$$f_{DEV} = \frac{BW}{number\ of\ steps} \quad (7)$$

$t_{step_{min}}$ is the minimum time PLL needs to step from one frequency to the next, so t_{step} is a multiple of $t_{step_{min}}$. Using equation 5, choose the appropriate values of CLK1 and CLK2 to get the desired t_{step}. In our case, we chose $t_{step} = t_{step_{min}} = 50ns$, so CLK1 = CLK2 = 1. Then from equation 6 and using T = 0.7ms, number of steps = 14000, and from equation 7, $f_{DEV} = 5714\ Hz$.

The following equations are needed to calculated DEV and DEV_OFFSET.

$$f_{DEV} = \frac{f_{PFD}}{2^{25}} * DEV * 2^{DEV_{OFFSET}} \quad (8a)$$

$$DEV_{OFFSET} = \frac{log_{10}(\frac{f_{DEV}}{f_{RES} * DEV_{max}})}{log_{10}(2)} \quad (8b)$$

First you will need to calculate DEV_{OFFSET} using equation 8b by setting $DEV_{max} = 2^{15}$ and use the values you calculated before. After you calculated for DEV_{OFFSET}, plug the value into equation 8a to find DEV.

After calculating all these values, follow the timing diagram on the datasheet to set the corresponding registers to the desired values.